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CMOS interface circuits for spin tunneling junction based magnetic random access memories
by

Ganesh Saripalli

> A thesis submitted to the graduate faculty in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE

Major: Computer Engineering<br>Program of Study Committee:<br>William C. Black Jr., Major Professor<br>Art Pohm<br>John E. Snyder

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This is to certify that the master's thesis of Ganesh Saripalli has met the thesis requirements of Iowa State University

Signatures have been redacted for privacy

## DEDICATION

This small piece of work is dedicated to my parents S.Sathyavani and S.SomaSundaram. I feel extremely indebted to the Almighty for giving me enough strength to finish my Masters degree successfully.

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## ABSTRACT

Magneto resistive memories (MRAM) are non-volatile memories which use magnetic instead of electrical structures to store data. These memories, apart from being nonvolatile, offer a possibility to achieve densities better than DRAMs and speeds faster than SRAMs. MRAMs could potentially replace all computer memory RAM technologies in use today, leading to future applications like instant-on computers and longer battery life for pervasive devices. Such rapid development was made possible due to the recent discovery of large magnetoresistance in Spin tunneling junction devices. Spin tunneling junctions (STJ) are composite structures consisting of a thin insulating layer sandwiched between two magnetic layers. This thesis research is targeted towards these spin tunneling junction based Magnetic memories.

In any memory, some kind of an interface circuit is needed to read the logic states. In this thesis, four such circuits are proposed and designed for Magnetic memories (MRAM). These circuits interface to the Spin tunneling junctions and act as sense amplifiers to read their magnetic states. The physical structure and functional characteristics of these circuits are discussed in this thesis. Mismatch effects on the circuits and proper design techniques are also presented. To demonstrate the functionality of these interface structures, test circuits were designed and fabricated in TSMC $0.35 \mu$ CMOS process. Also circuits to characterize the process mismatches were fabricated and tested. These results were then used in Matlab programs to aid in design process and to predict interface circuit's yields.

## 1 INTRODUCTION

### 1.1 Motivation

The field of Magneto-resistive random access memories (MRAM) has experienced significant development ever since they were introduced two decades ago [2]. Continued research efforts in this field have helped them compete with the faster and denser semiconductor random access memories, making them a potentially attractive solution for future memory applications. These memories were initially targeted to replace early non-volatile memory technologies like Ferrite cores and Plated wire, because these have infinite read/write endurance and need less energy to write, making them a favorable solution for even high-speed re-programmable systems.

Successful working models of magneto-resistive memories have been demonstrated in the past $[3,4,5,6,7,8]$ using either Anisotropic Magneto-resistance effect (AMR) or Giant Magneto-resistance effect (GMR). These memories, even though successful, could not compete with the semiconductor RAMs due to slower read speeds. The amount of magneto-resistance available was not high enough for successful application (typically $6 \%$ in GMR, $2 \%$ in AMR); resulting in small input signal levels for the sense circuits. This resulted in large access times and also degradation in the signal-to-noise ratio. But ever since the discovery of Spin tunneling junctions in 1995 [9], application of these devices in MRAMs is a great opportunity to compete with contemporary semiconductor memories. Spin tunneling junctions are inherently high impedance devices and demonstrated a large magneto-resistance effect of nearly $40 \%$ in certain cases [10, 11]. Due to these characteristics, MRAMs based on spin tunneling junctions may have comparable input signal levels $(20 \mathrm{mV})$ on par with semiconductor memory elements; and thus should
run at comparable speeds. Considerable research activities are being done today in the industry to build a successful Spin tunneling junction based MRAM to ultimately compete with the speeds of SRAM and densities of DRAM.

Given these physical merits of SDT (Spin dependent tunneling) devices, several simple memory cell architectures using SDT devices as non-volatile storage can be conceived. In this thesis, four such types of structures are proposed. Test circuits for these structures had been designed and fabricated in TSMC $0.35 \mu$ CMOS technology. The behavioral and structural characteristics of the proposed structures will be explained and analyzed in detail. And also the various test results for the designed circuits will be presented and interpreted.

### 1.2 Thesis Organization

To better understand the complete working of these memory interface circuits, detailed analysis of the SDT devices is essential. Chapter 2 gives an overview of the spin tunneling effect and the various types of SDT devices available. The structural details and functional characteristics of such devices will be described. Also the special hybrid memory structure used in this thesis will be explained in detail.

Chapter 3 gives the complete details of all the four proposed memory interface circuits. The design and functionality of these structures will be elaborated. And also the merits and shortcomings of each memory structure will be discussed.

In chapter 4, certain design consideration and process mismatches are introduced. Mismatch effects cause huge degradation in the performance of these memory circuits. Hence the various types of mismatches present and their effects will be investigated. Also mismatch measurement circuits and their test results are explained in detail.

In Chapter 5, measurement results of all the proposed test structures will be presented. Wafer level testing setup and test result inferences will be elaborated. Finally, the contributions of this research and some future work will be presented as conclusion part in chapter 6 .

## 2 SDT DEVICES

Spin Dependent Tunneling (SDT) devices are thin film trilayer structures, with two ferromagnetic layers sandwiching a nanometer thick non-magnetic insulator layer. This chapter gives an overview of the basic composition and functionality of a typical spin dependent tunneling device. Also the special type of Hybrid Spin dependent tunneling structure used in this thesis will be described in detail.

### 2.1 Spin Dependent Tunneling

Tunneling naturally occurs when a voltage is applied between any two metals separated by a thin dielectric and is found to be a linear function of the applied voltage (the relationship is actually exponential in nature, but can be approximated by a linear function when the applied voltage is small). But when the metals are ferromagnetic, then an additional barrier is introduced for the tunneling electrons, and which is spin dependent. This phenomenon where the tunneling current is dependent on the spin direction of the conducting electrons is known as Spin Dependent Tunneling (SDT) effect.

### 2.1.1 SDT Effect Overview

The reason for such spin dependent tunneling is due to the specific conducting properties of ferromagnetic (FM) films. Any FM film possesses an inherent magnetic moment, caused by unequal filling of energy bands at the Fermi level. Such an imbalance leads to a spin polarized current mechanism throngh them, causing them to favor electrons of one Spin State to another Spin State. So depending upon the electron's spin direction, a FM film can either art as a condurtor or as an insulator. This property of the FM
films is characterized by a polarization constant, given in equation 2.1 [12].

$$
\begin{equation*}
P=\frac{n \uparrow-n \downarrow}{n \uparrow+n \downarrow} \tag{2.1}
\end{equation*}
$$

where $n \uparrow$ are number of carriers with spin up, and $n \downarrow$ are number of carriers with spin down. Ideally we would like to have $100 \%$ polarized materials which exhibit pure digital states of electron conduction. But present day FM films have P around $40 \% \sim 50 \%$, adequate enough to realize useful devices.

Thus when two FM films are separated by a thin dielectric, electrons of that spin state favored by both films are more likely to tunnel through the barrier while the other electrons tend to get stopped. And since magnetic moments of the FM films indicate their polarization, we can as well say that the tunneling probability of electrons is higher when the two magnetic moments are parallel to each other than when they are anti-parallel. This then leads to the spin dependent nature of the tunneling current in any SDT structure.

Spin dependent tunneling devices are current-perpendicular-to-plane (CPP) structures, meaning the tunneling current is perpendicular to the plane of the ferromagnetic films. As explained above and given in figure 2.1, the tunneling current is observed to be a strong function of the difference between the two magnetic moment orientations $(\phi)$. This change in the tunneling current with magnetic moment orientation can be correlated to a macroscopic magneto tunneling resistance, which can be modeled as shown in equation 2.2 [13]

$$
\begin{equation*}
\frac{\Delta R_{\max }}{R_{0}}=\frac{R_{a p}}{R_{p}}-1=2 \frac{P_{1} P_{2}}{1-P_{1} P_{2}} \tag{2.2}
\end{equation*}
$$

where $R_{p}$ is the junction resistance for parallel alignment of magnetic moments, while $R_{a p}$ the resistance for anti parallel alignment, and $P_{1}$ and $P_{2}$ are the spin polarization of the two ferromagnetic layers. Note that equation 2.2 does not take into account many limiting factors like coupling and surface degradation in the FM films, and hence represents the maximum resistance obtained in the ideal case. A more practical representation of the nominal resistance and the resistance change with respect to $\phi$ is given
in equations 2.3 and 2.4 [14]

$$
\begin{align*}
R_{0} & \approx\left(K_{1} S\right) e^{\left(K_{2} S\right)}  \tag{2.3}\\
R & \approx R_{0}-\frac{\Delta R_{\max }}{2} \cos (\phi) \tag{2.4}
\end{align*}
$$

where $K_{1}$ and $K_{2}$ are material constants and ' S ' is the tunneling barrier thickness.


Figure 2.1 Tunneling junction resistance as a function of magnetic moment orientation

### 2.1.2 SDT Structure

The basic structure of a typical spin dependent tunneling device is shown in figure 2.2. The ferromagnetic layers are of $10-30 \mathrm{~nm}$ thick, while the non-magnetic insulator layer is typically 1-2 nm thick. Earlier experiments on spin dependent tunneling [13], used amorphous $\mathrm{Ge}(100 \AA$ thick $)$ or $\mathrm{NiO} / \mathrm{Al}_{2} \mathrm{O}_{3}$ ( $150 \AA$ thick) as interface layers, while the two ferromagnetic layers were of Co and NiFe respectively. But such structures hardly gave $2-4 \%$ magneto-resistance change at room temperature and were further reduced with any bias voltage applied. Hence these structures did not prove to be any useful device.

But the recent discovery of spin dependent tunneling at room temperatures [9] in 1995 demonstrated considerable magneto-resistance change of $11.8 \%$ at 295 K and $24 \%$ at 4.2 K . This was tested on a $\mathrm{CoFe} / \mathrm{Al}_{2} \mathrm{O}_{3} / \mathrm{Co}$ structure, where the alumina barrier was grown to $16-18 \AA$ thick, while the other two ferromagnetic layers of $\mathrm{CoFe} / \mathrm{Co}$ were of $80 \AA$ and $300 \AA$ respectively. The increase in $\left(\frac{\Delta R}{R}\right)$ was attributed to the decrease in surface roughness of the ferromagnetic layers, in addition to choosing good tunneling


Figure 2.2 Basic structure of a Spin Dependent Tunneling (SDT) device

Most of the tunneling devices, which are built after this discovery, are based upon the same type of structure composition. The tunneling barrier is predominantly alumina, with a few variations in the ferromagnetic layers. But nonetheless, the idea was to use an insulating material as the non-magnetic layer, to achieve the desired higher resistance for the overall structure.

### 2.1.3 Spin Valve and Pseudo Spin Valve SDT Devices

SDT structures, similar to GMR devices, can be classified into two main types Spin valve SDT devices and Pseudo Spin Valve SDT devices. Both of these share a similar physical structure but are different in their methods of storing data. Spin valve devices, consists of a pinned ferromagnetic layer whose magnetic moment is fixed in a predetermined direction, while Pseudo spin valve device has both its layers UN-pinned (i.e) whose moments are free to rotate.

Figure 2.3 shows a typical spin valve SDT structure, along with a orthogonal word line. The magnetic field produced by the current passing through the word line is used for switching the soft layer's magnetic moment. Thus by varying the word current's direction, we can either align or anti-align the soft layer's magnetic moment with the hard layer's magnetic moment. And thereby vary the tunnel junction's resistance. Figure 2.4 [15] shows the R-H characteristics of this structure, where the magnetic field produced by the word current is represented as X-axis. As shown in the figure, parallel alignment
of the magnetic moments results in lower resistance than the anti-parallel alignment. The traces in the graph represent the direction of word current variation. Also shown, is the $H_{s a t}$ (or) Saturation word field, which is the field required for switching the hard layer's magnetic moment. So if we keep increasing the word field above $H_{s a t}$, both layer's magnetic moments come into alignment resulting again in lower resistance. Thus the word current's range is restricted by $H_{s a t}$ values to realize higher resistance states.


Figure 2.3 Spin valve tunneling junction structure


Figure 2.4 R-H characteristics of spin valve tunneling junction

Figure 2.5 shows the physical structure of a pseudo spin valve SDT structure. It is very similar to a spin valve device except for the absence of an anti-ferromagnetic layer. Under the absence of any external magnetic fields, the structure ideally stays in its stable state with both moments in anti-parallel or parallel alignment (refer to figure 2.5). When current is passed through the word line, a magnetic field is produced which may be used to switch one or both of the layer moments. Even though both the layers are free to rotate, usually one of the layers is made harder to switch. This difference in
the coercitivities is achieved by varying the thickness or composition of the two lavers. Hence the behavior of a pseudo spin valve is similar to a spin valve device characteristics, but we actually have 4 different states during typical operation instead of 2 states as in spin valve devices. Figure 2.6(a) and 2.6(c) show, what are called as "major loops", when the word field is changed all the way in one direction. As the word current changes from left to right as shown in figure 2.6(a), the thin film stays in the low resistance state until the word field is large enough to overcome the switching threshold of the "softer layer" and rotate it to the right. Anti-parallel alignment results in a high resistance-state. As the word field keeps increasing, the generated field eventually becomes large enough to rotate the moment in the "harder layer". The moments in both layers are now pointing to the right;lower resistance-state is exhibited. For the opposite case, when the word field is changing from right to left as indicated in figure 2.6(c), the same situation as the previous case occurs, but the switching fields required are different.

As shown in figure 2.6(b) and (d), a different phenomenon occurs when the thin film is biased from low-resistance state to high-resistance state. When the word current flips the "softer layer" to anti-parallel alignment and then rotates it back to parallel alignment, the resistance curve of the thin film does not follow the same low-resistance-to-high-resistance trace. Instead a hysterisis curve is displayed when the alignment is brought back to parallel alignment. These loops are termed as minor loops.


Figure 2.5 Pseudo spin valve tunneling junction structure


Figure 2.6 R-H characteristics of pseudo spin valve tunneling junction

### 2.2 Hybrid SDT/Magnetic Sandwich Device

The spin dependent tunneling magneto-resistive structure used for our experiments was a hybrid structure pioneered by Non-volatile electronics (NVE) corporation, MN, USA. Figure 2.7 (courtesy of [16]) shows the laver composition of such a structure. It is a composite design made up of a spin tunneling junction realized on top of a magnetic sandwich.

### 2.2.1 Why Hybrid Device?

Traditionally Magneto-Resistive random access memories (MRAM) have been realized using 2-Dimensional (2D) selection approach, where the magnetic elements are arranged in a X-Y grid and the bit selection is realized using two orthogonal word lines. Fig 2.8 shows a typical 2D MRA.M arrangement. corresponding to any type of magnetic memory (AMR, GMR. SDT) element used. The word lines carry "half-select" currents, meaning the current in one word line prodnees half the field required to reverse a soft


Figure 2.7 Structure of hybrid SDT/magnetic sandwich device
layer's magnetic moment. Hence wherever the two word lines intersect, the overall field from both word lines will be sufficient to reverse the underneath selected magnetic bit. The half field produced elsewhere supposedly should not affect the other magnetic elements. The main advantage of such a approach is higher density, since we do not need extra transistors to select the magnetic bits.


Figure 2.8 2D selection scheme for the grid-type memory array

But the 2 D approach fails under many circumstances, mainly due to the lack of uniformity in magnetic bit's switching thresholds and due to varying disturb characteristics of the half-select currents. One solution to this problem is to use a 1D-selection scheme, where we use a transistor for each of the magnetic elements to enable bit selection. Fig
2.9 (courtesy of [16]) shows the desired 1D selection scheme. Both reading and writing of magnetic bits is accomplished by enabling the select transistor, but varying the magnitude of current through the transistor. Thus even though we still have a 2D array of the magnetic elements, the selection of the bits is done using a single access transistor. And hence this scheme is called as 1D magnetic selection approach.


Figure 2.9 1D selection scheme for magneto-resistive cells

The limitations of using a normal spin dependent structure in a 1D approach, is due to the large amount of required write current $\simeq 2-3 m A$. There is a potential danger of damaging the magnetic bit, when such high currents are conducted through the tunnel junction. To overcome this difficulty, we need to separate the writing path of the spin tunneling junction from its read path; but still maintain the 1D selection approach to limit the number of access transistors. The new structure proposed by NVE promised these goals, by using a spin tunneling junction for maintaining high readout signals, but a separate magnetic sandwich beneath the tunnel junction for conducting the huge write current. And also only a single access transistor is used for enabling the 1 D selection scheme, as shown in figure 2.7 .

### 2.2.2 Structure

The complete detailed structure of magnetic sandwich bit is shown in figure 2.7. The bottom 3 layers form the magnetic sandwich used to conduct the large write currents. Both the permalloys are UN-pinned, and have their magnetic moments lying across
the strip. Under the absence of any external field, the magnetic moments in the two permalloys align in anti-parallel direction always. And by passing the write current through the stripe we can alter the direction of both the magnetic moments. Having both layers as UN-pinned helps in reducing the stray magnetic fields produced by the huge write currents. The non-magnetic layer in the sandwich can be a conductor like Cu or an insulator like Alumina, but using a good conductor helps increasing the coupling of the two permalloys.

The spin-tunneling junction is formed between the top pinned layer and upper permalloy layer of the magnetic sandwich. Thus by changing the direction of upper permalloy layer's magnetic moment, we can control the amount of tunneling magnetoresistance by either aligning or by anti-aligning with the pinned layer. The pinned layer is a composite structure, realized by sandwiching a thin ruthenium layer by two magnetic CoFe layers. And the top CoFe layer in this structure is pinned by an anti ferromagnetic layer. Both the CoFe layers are approximately of the same thickness. Such a structure has a strong anti-parallel alignment and thus produces very low stray magnetic fields. The tunneling barrier is realized as usual in alumina.

### 2.2.3 Behavior

Writing of this bit is achieved by passing a large write current through the magnetic sandwich. The magnetic field produced by this current will be in opposite directions in both permalloys, as shown in figure 2.7. Thus it facilitates us to write either a "1" or " 0 ", either the top film magnetized to the left and the bottom to the right, both being perpendicular to the current direction, or vice versa. Cells on the order of micron width were found to need a write current of $\simeq 2.5-5 m A[1]$.

Reading is accomplished by passing a constant current through the magnetic tunnel junction. Thus depending upon the amount of magneto-resistance present, the output voltage will be either high or low, and when compared to a reference voltage, the logic state can be easily detected. This bit structure when connected to a single transistor, as shown in figure 2.7, will then become a single cell in the 1D MRAM approach. A

Table 2.1 Qualitative comparison of the hybrid structure with other technologies (courtesy of [1] )

| Device | Write Current | Ease of Mfg. | Speed | Density |
| :--- | :---: | :---: | :---: | :---: |
| PSV | 25 mA | Harder | Medium | High |
| SDT | 25 mA | Harder | High | Medium |
| HYBRID CELL | 2.5 mA | Easier | High | Low |

separate access transistor is also connected to the tunnel junction to read the sensed output voltage. A $40 \%$ [1] magneto-resistance had been demonstrated with a 100 mv bias voltage across the barrier, thus producing 40 mv signal output. The tunneling barrier resistance was high enough to limit the tunneling current to around $20 \mu \mathrm{~A}$. Table 2.1 (courtesy of [1] ) gives a performance comparison between a traditional PSV (pseudo spin valve) cell and a spin tunneling junction (SDT) used in a 1D approach, compared to that of the hybrid structure.

From the above table, we can see that the hybrid structure has many advantages compared to the other technologies in terms of the speed and manufacturability. The only limitation is of the density, because of the bigger size of the hybrid structure. However for smaller memories, this limitation is surpassed by the overhead space required for the peripheral pads and interface circuits. Hence for smaller density memories, hybrid structure has the clear advantage over the others and thus motivated us to use in our research.

## 3 IMPLEMENTATION DETAILS

In any MRAM structure some kind of a sensing mechanism has to be built in order to read the state of the magnetic bits and output the respective logic levels. Different possible methods of implementing such an interface have been proposed in the past [ 6, $8,16,1]$. In this thesis, we have implemented one particular style of interface mechanism using CMOS differential amplifier circuits as the sensing elements. The main focus of this chapter would be to explain the detailed design and behavior of all the proposed interface circuits.

### 3.1 Basic SDT MRAM Sensing Schemes

There are different mechanisms of sensing the magnetic bits, but we can group most of them into three basic categories:

- Non-destructive 2-Dimensional(2D) readout mechanism
- Single transistor 1-Dimensional(1D) access mechanism
- Differential resistor sense amplifier mechanism

The traditional 2D approach, as mentioned in the previous chapter, consists of an XY grid placement of the memory bits. Each memory bit is overlaid with two other word lines in an orthogonal fashion, used for both reading and writing purposes. Reading is accomplished by passing a low current through the selected spin-tunneling junction and by detecting the corresponding voltage change across it. The voltage observed should be a linear function of the bit resistance and hence denotes the magnetic bit's state. Even though this approach has the highest possible memory density, it suffers from
certain limitations. The non-uniformity in the switching fields and disturb sensitivity of the memory bits, causes this approach to have very low yields. Moreover, the memory states induced due to the half-select write currents are very unstable and might cause cell failures in the long run.

The single transistor 1D approach consists of a similar X-Y grid layout but without any orthogonal word lines. Each tunneling junction is provided with a single transistor acting as the access element. Hence the selection of memory bits is now done using a single transistor instead of a complex word line grid. Both reading and writing is accomplished by passing the appropriate amount of current through the accessed spintunneling junction. The advantage of such a scheme is the simplicity of its sensing mechanism but it comes at a cost of reduction in the density.

In both the above mentioned methods, the amount of input signal obtained is less, thereby limiting the circuit's response speed. Also they require large amount of read/write current to operate, leading to higher power consumption. Due to these limitations, both methods are not favored much. For magneto-resistive memories to compete with semiconductor memories, they should have high speed and low power consumption. The third method of differential resistor sense amplifier technique satisfies these requirements - by employing differential technique to double the input signal and amplifier structures to boost the speed thereby reducing the amount of read current required and in turn the power consumed.

Differential resistor sense amplifier is similar to a static RAM cell, except that the memory elements are now spin tummeling junctions. Similar to any typical memory sense amplifier, a differential signal is reguired. In order to provide the necessary input, two spin tunneling resistors are emplowed as the differential input source and also as the non-volatile storage unit. To serve as the differential signal source, the two resistors have to be always in the states that are opposite to each other; i.e., one resistor must display a high resistance state while the other low resistance at the same time. This differential topology not only helps in doubling the signal level but also enhances the common mode rejection in the cirmit

### 3.2 Circuit Requirements

Apart from the differential topology, the proposed interface circuits had to meet some key requirements due to the usage of spin tunneling junctions :

- Must protect the spin-tunneling junctions from over voltage. The magneto-resistance obtained from a tunnel junction reduces drastically above a certain bias voltage. And also applying large voltages across the tunnel junction might cause pin-holes in the tunneling barrier thus leading to the complete destruction of magnetic bit. Usually this upper limit varies from $100 \mathrm{mV} \sim 150 \mathrm{mV}$. So the interface circuits had to restrict the voltage drop across the spin-tunneling junctions while sensing is done.
- Minimize the effect of Spin tunneling junction's time constant to increase the sense speed. And should also have small sense current for reducing the power consumption. This will be explained in detail in the next section, where the spin tunneling junctions are modeled.
- Should have minimal external interface and thus should include both the read/write circuitry for memory bits. Hence all the interface circuits designed will have an additional circuit block meant for writing the SDT magnetic bits into desired memory states.


### 3.3 Spin Tunneling Junction Modeling

All the interface circuits designed in this thesis used the special hybrid magnetic tunneling device developed by NVE Corporation. The amount of magneto-resistance available was $10 \% \sim 40 \%$, and the nominal tunnel junction's resistance-area product (RAP) was around $200 K \Omega-\mu m^{2}$. The write current required to properly write the magnetic sandwich was around $4 m A \sim 5 m A$.

The tunnel junction's RAP is highly dependent on the uniformity of its tunneling barrier. Since there could be a lot of process related variation, worst case deviations of

Table 3.1 Nominal resistance ranges used in the simulations

| cases | Nominal Resistance | Resistance variation | Nominal $\bar{I}_{\text {sense }}$ |
| :--- | :---: | :---: | :---: |
| Case 1 | $25 K \Omega$ | $10 K \Omega \sim 50 K \Omega$ | $3 \mu A(150 \mathrm{mV} / 50 K \Omega)$ |
| Case 2 | $75 K \Omega$ | $30 K \Omega \sim 150 K \Omega$ | $1 \mu A(150 \mathrm{mV} / 150 K \Omega)$ |
| Case 3 | $200 K \Omega$ | $150 K \Omega \sim 250 K \Omega$ | $0.5 \mu A(150 \mathrm{mV} / 250 K \Omega)$ |

around $100 \%$ were assumed for the tunnel junction's resistance. Hence for a nominal resistance of $50 \mathrm{~K} \Omega$, the resistance variation was assumed to be anywhere from $25 \mathrm{~K} \Omega \sim$ $100 K \Omega$. Moreover, in order to demonstrate the proof of concept, the interface circuits were designed for a broader range of tunneling resistance. Three values of nominal resistance were chosen in the range, depending upon the amount of sense current $\left(I_{\text {sense }}\right)$ required; in order to keep the voltage across the magnetic bits less than 150 mV . Also the magneto-resistance value ( $\Delta R$ ) was assumed to vary anywhere from $10 \%$ to $40 \%$, hence simulations were done at three values of magneto-resistances $(\Delta R)$ of $10 \%, 25 \%$, and $40 \%$. Table 3.1 shows the details of the three cases.

In order to perform simulations of the interface circuits, we had to model the spintunneling junction. A simple voltage controlled resistor (VCR) was used for modeling the tunnel junction's resistance variation. The reason for using a VCR was to facilitate changing the state of tunneling junction, with the use of a simple voltage source. By doing so, we can easily automate the magnetic bit's writing process into the simulations. This aspect will be explained in detail later when the simulation environment is explained. The magnetic sandwich of the hybrid structure also contributes some resistance and hence a simple resistor was used to model it.

The spin-tunneling junction has an inherent RC time constant due to the presence of a parasitic capacitance between the two ferromagnetic layers. This capacitance is the major factor in reducing the speed of the tunnel junctions, and hence had to be included in simulations for proper results. The value of the parasitic cap is calculated by assuming a parallel plate capacitance between the two ferromagnetic layers; calculated using the thickness and relative dielectric constant of the insulator layer. A sample calculation is
as follows

$$
\text { Permittivity of } \begin{align*}
\mathrm{Al}_{2} \mathrm{O}_{3}, \varepsilon & =8 \times 8.85 \times 10^{-12} \mathrm{~F} / \mathrm{m}^{2} \\
\Rightarrow C_{o x} & =\varepsilon \times \frac{\text { Area }}{s} \tag{3.1}
\end{align*}
$$

where 's' is the thickness of the tunneling junction. For a dielectric thickness of $15 \AA$ and a typical area of $1 \mu m^{2}$ [17], we get a nominal value of 50 fF for the parasitic capacitance. Figure 3.1 shows the complete model of the hybrid structure used in our simulations. The sandwich resistance was split into two resistors for clarity purposes, and thus does not hold any significance.


Figure 3.1 Simulation model for hybrid magnetic structure

Since we need differential resistors, we need to write the two hybrid structures in opposite manner. This can be accomplished by connecting the magnetic sandwiches in either series or in parallel fashion, as shown in the figure 3.2. But using the series connection reduces the amount of complexity, since we now need one single metal line for write current pulse. Hence by doing so, a single write current pulse would be sufficient to orient the two magnetic structures into differential phase. Also shown in the figure is the complete simulation model used for the two magnetic resistors, obtained by connecting the sandwich resistor legs of the two individual VCR models. Note that the control voltage of the two VCRs would be now in opposite phase, to model the differential writing.


Figure 3.2 Two methods of writing the differential magnetic bits

### 3.4 Magnetic Bit Write Circuitry

Since we wanted our interface circuits be complete, some kind of write circuitry had to be included along with the magnetic bits. The function of this control circuitry is to direct the word current in the correct direction depending upon the state into which the magnetic bits are written. The complete schematic is shown in figure 3.3. The R/W signal controls the read or write phase, and has to be low for the write phase to start. The Write10 signal controls the Logic state into which the resistors are written. When Write10 is high, R1 (left resistor) is written high/low (depending upon the pinned layer's magnetic moment direction) and R2 (right resistor) is written low/high respectively and vice versa when Write10 is low. Figure 3.4 shows the two phases of the control circuit, highlighting the write current direction and the corresponding conducting transistors.

During read phase, we need to ground the write current path or in other words, the magnetic sandwiches of the two hybrid structures. This was done using the three additional transistors included in the complete write control circuit. Ref node corresponds to the series intermediate connection between the two magnetic sandwiches.


Figure 3.3 Magnetic bit write circuitry

The circuit was designed to conduct a maximum current of 5 mA for worst case condition. The nominal value of the sandwich resistance was assumed to vary around $100 \Omega \sim 200 \Omega$. Under this assumption, there will be a worst case voltage drop of 2 V $(5 m A \times 200 \Omega)$ across the magnetic sandwich. Given these specifications, the transistor sizes were appropriately calculated and adjusted for proper functionality. All the conducting transistors would be operating in triode region, and are designed to have minimum vds drop across them. Table 3.2 gives the sizes of the various transistors used


Figure 3.4 Different writing modes in the magnetic bit write circuitry

Table 3.2 Device sizes in the magnetic bit write circuitry

| Device ID | Design Size (W/L) |
| :--- | :---: |
| M1,M2 | $32 \mu / 0.5 \mu$ |
| M3,M4 | $90 \mu / 0.5 \mu$ |
| M5 | $80 \mu / 0.5 \mu$ |
| Shorting transistors, M6,M7\& M8 | $5 \mu / 0.5 \mu$ |

in the write control circuit.

### 3.5 Interface Circuits

All the interface circuits were designed in TSMC $0.35 \mu$ process. In designing the interface circuits, two foremost design specifications had to be satisfied for the proper functioning of circuits. First, the voltage across the resistors or magnetic tunnel junctions should be restricted below 150 mv under all conditions and process corners. And second, the output voltages should come to correct logic level depending upon the state of the magnetic bits. The difference in the various interface circuits described here lies in the manner we meet these two specifications. Hence in explaining the interface circuits, more stress will be laid on these two design aspects. Moreover, in all these designs, bit write circuitry was also included for completeness in the simulation.

### 3.5.1 Interface Circuit-I

Figure 3.5 shows the complete schematic of this interface circuit. The design was done for all the ranges of magnetic resistance and hence according to table 3.1 three different schematics were constructed. The following sections explain in detail the complete construction and functionality of this interface circuit

### 3.5.1.1 Structure

The first design requirement was met by using a constant bias circuit to restrict the voltage across the magnetic bits. The transistors $\{\mathrm{M} 8, \mathrm{M} 9\}$ and resistor $\{$ biasR $\}$ (refer


Figure 3.5 Schematic of interface circuit-I
to figure 3.5) form the complete bias circuit. It is based on the principles of replica biasing, since the bias leg is a replica of the NMOS path $\{\mathrm{M} 4, \mathrm{M} 2$, magnetic resistor R2\} in the interface circuit. Thus by having a replica, if we can restrict the voltage across the bias resistor, then the voltage across the other two resistors (or) magnetic tunnel junctions is also restricted.

The bias circuit used, in a sense is not a "true" replica bias configuration, since we did not use a magnetic resistor in the bias leg. Instead a polysilicon resistance was used for realizing the same. The reason for doing so was that the variations in the Resistancearea product of the magnetic tunnel junction are expected to be huge and greater than the process variations in the poly resistance. Since the bias resistor is the determining factor in restricting the voltage across tunnel junctions, it is preferred not to have large process variations in this resistor. Moreover, the bias resistance was designed to be a nominal average of the two differential resistors. Since the hybrid structure can be either in high resistance state or low resistance state, it is difficult to realize an average value using a single hybrid magnetic resistor. Nonetheless the underlying concept is the same; whether we use a poly resistor or a magnetic resistor for biasing. Hence by restricting the voltage across the poly resistor below 150 mV under all conditions, we could ensure
the correct working of the magnetic bits.
The second requirement of correct logic state sensing was done using a PMOS current mirror formed by transistors $\{\mathrm{M} 5, \mathrm{M} 6\}$. The current mirror configuration acts as a high gain amplifier to any current difference between the two legs. Hence the current difference induced by the differential magnetic resistors, gets amplified by the current mirror and is reflected in the outputs $\left\{\right.$ Out $_{1}$, Out $\left._{2}\right\}$ as proper logic levels. Simulations were performed under all process corners, verifying the above two requirements.

The transistors $\{\mathrm{M} 1, \mathrm{M} 2\}$ are enable transistors controlled by the "RWen" (Read/Write Enable) signal. These transistors serve two purposes:

- To disconnect the interface circuit during writing of the magnetic bits, in order to avoid wrong logic states to be latched at the output.
- To serve as an aid in reducing the voltage spikes on the magnetic tumeling junctions during writing of the bit. This can be explained by looking at figure 3.6, where the magnetic tunneling resistor is shown along with its parasitic cap and also the Cgs cap of the enabling transistor. When the write current pulse is introduced, due to the series connection of the two parasitic caps, most of the voltage gets dropped across the smaller Cgs cap instead of the other capacitance, as calculated in the figure. If these enable transistors had not been there, the entire voltage spikes would have appeared across the magnetic tunnel junction. And since these voltages $(\approx 1 V \sim 2 V)$ are much larger than 150 mV , the tunnel junction could have easily been destroyed. Hence by including these enable transistors, we were able to protect the magnetic tunneling junctions from over voltage spikes.

Apart from all these, extra buffers are added to the interface circuit outputs, in order to get the full rail-to-rail swing. The extra PMIOS transistor M7 was added to correct one inherent problem of this interface circuit. and will be explained later. But the main function of this transistor was to ensure the correct latching of final outputs during the write phase.


Figure 3.6 Reduction of voltage spikes across the tunnel junction

### 3.5.1.2 Functionality

The working of this interface circuit can be explained by considering the interaction between the top PMOS and bottom NMOS current paths of the circuit. Since equal bias voltage is applied to the two NMOS paths, a difference in the NMOS currents is introduced due to the differential resistor configuration. And since the PMOS current mirror section tries to keep equal current in the two legs, an imbalance occurs between the pull-up and pull-down currents at the output nodes. This current imbalance then helps in bringing the output nodes to the correct potential reflecting the magnetic bit's states.

Now consider the case where $R 2$ (right resistor) $\geq R 1$ (left resistor) [refer to figure3.5]. Since equal bias voltage is being applied on both resistors, the current through $R 2$ becomes lesser than through $R 1$. But due to the current mirror configuration of $M 5 \& M 6$, the current through $M 6$ is made equal to the current through $R 1$ [which is the same as through M5]. This then leads to the situation, where instantaneously the pull up current through $M 6$ will become greater than the pull down current through $R 2$, causing the $O u t_{2}$ node to be brought towards $v d d$. Thus the $O u t_{2}$ node is made to reflect the correct state of the magnetic bits. The vice versa situation of $R 1 \geq R 2$ is also based on similar lines, but in which case the $\mathrm{Out}_{2}$ node will then be brought down towards
ground potential.
Even though we have two output nodes, $O u t_{2}$ is the true output when compared to Out ${ }_{1}$ [refer to figure 3.5] node. Since M5 is diode-connected, the $V_{d s}\left(=V_{t h}+V_{d}^{\text {sat }}\right)$ drop is higher on M5 compared to the $V_{d s}$ drop of M6. Hence the voltage swing obtained from the $\mathrm{Out}_{2}$ node is higher than that obtained from the $O u t_{1}$ node, making it sufficient enough to dictate the proper logic functionality. Therefore, only $O u t_{2}$ node is to be tested for determining the working of this interface circuit. But note that output buffers were added to both the output nodes, to maintain symmetry in the circuit.

Figure 3.7 shows the simulation results proving the proper working of this interface circuit. As can be seen from the figure, the SDT bits are flipped alternatively by the write01 signal and the output node $O u t_{2}$ reflects this state correctly.


Figure 3.7 Simulation results of interface circuit-I

Table 3.3 Device sizes used in interface circuit-I

| Device ID | Design Size (W/L) |
| :--- | :---: |
| M1, M2, M9 | $0.5 \mu / 0.5 \mu$ |
| M3, M4, M8 | $0.5 \mu / 0.5 \mu$ |
| M5, M6 | $0.5 \mu / 4 \mu($ for Bias resistance $=25 K \Omega$, |
|  | $75 K \Omega), 0.5 \mu / 8 \mu($ for $200 K \Omega)$ |
| M7 | $0.5 \mu / 0.5 \mu$ |

### 3.5.1.3 Design Considerations

There were a couple of design considerations that had to be taken care of:

- Addition of the PMOS transistor M7: As said before, it is used to drive the final outputs into correct state while writing of the magnetic bits. At the start of the write phase, the magnetic resistors are cut off from the interface circuit. Hence, in the absence of M7, the output nodes are pulled up towards Vdd (due to larger PMOS currents) and due to the finite charging time of the nodes, the output voltages come into intermediate logic levels. In order to avoid these indeterminate logic levels, M7 was added to act as strong pull-up path for the output nodes. Hence it was added to the true output node $\mathrm{Out}_{2}$ and controlled by the RWen signal. Thus the $O u t_{2}$ node is pulled up to Vdd logic level when in writing phase and the intermediate unknown logic levels are avoided.
- Layout Considerations: All the transistors are of minimum size width/length in the interface circuit except for the PMOS current mirror transistors. Guard rings were added wherever possible to prevent latch-up formation and also to isolate the bias resistance from any digital switching noise. The layouts of this interface circuit along with the bit write circuitry is given in Appendix-A.

The final design parameters of this interface circuit once all the design considerations were taken into account, is shown in table 3.3

### 3.5.1.4 Merits \& Shortcomings

The main attractions of this kind of memory interface circuit are:

- It is very simple. It does not involve any separate pre-charge or reset phase as in traditional memory sense amplifiers. These can also be used as fuse replacement circuits or shadow memories that are only occassionally changed to variations on a D Flip-flop that must be quickly writable and readable.
- Due to its simple operation, the control logic involved in using these interface circuits in MRAMs is reduced. Thus making this interface circuit a very viable solution to traditional MRAM sensing methods.

But there are certain limitations to the performance of this interface circuit:

- Static power dissipation is present due to the constant bias circuit, when the interface circuit is active or in sense phase.
- The Cgs capacitance of the PMOS current mirror transistors is large and hence may load the output nodes. This can cause a potential reduction in the sensing speed of this interface circuit, by increasing the delay in the post-buffer output transitions.
- Mismatch in the NMOS transistors $\{\mathrm{M} 3, \mathrm{M} 4\}$ can cause an error in the output logic states. But due to the large resistance $(\approx 50 K \Omega-150 K \Omega)$ and magnetoresistance ( $\approx 20 \%-40 \%$ ) of the tunneling junctions, hopefully the mismatch effect in the threshold voltage should not affect the working of the interface circuit.


### 3.5.2 Interface Circuit-II

Figure 3.8 shows the complete schematic of interface circuit II. Here too, the schematics were designed for three ranges of magnetic resistance, as explained in table 3.1.


Figure 3.8 Schematic of interface circuit-II

### 3.5.2.1 Structure

The principles of design are very similar to the previous interface circuit, except for a variation in the sensing method. We use the same replica biasing scheme, as used in the first interface circuit, to restrict the voltages across magnetic tunnel junctions. Hence the transistor sizes used in the bias path are the same as previously designed.

The second requirement of correct logic state sensing is achieved through a combination of differential current mode sense amplifier and a latch. The two cross-coupled PMOS transistors $\{$ M5, M6\} serve the dual purposes. At the start of the sensing phase, these cross coupled pair act as a high gain amplifier, amplifying any current difference between the two legs. Once the difference in the two output nodes achieves a particular voltage level, the positive feedback kicks in and causes the two nodes to reach absolute voltage levels of Vdd and ground. Simulations were performed under all process corners, verifying the above two requirements.

An additional PMOS switch $\{\mathrm{M} 7\}$ is included in this interface circuit, to help regenerate the correct logic levels in each read cycle. The purpose of this switch is to short both the output nodes together and thus induce a current difference between the two
legs. This way, we make sure the previous state is removed and also help in sensing the correct logic states. Selection of this switch size needs careful attention in order to make the interface circuit work properly, and will be explained in detail in a later section. And similar to the first interface circuit, Read/Write Enable transistors $\{\mathrm{M} 3, \mathrm{M} 4\}$ and output buffers were also added.

### 3.5.2.2 Functionality

The sensing scheme of this interface circuit involves two phases
Reset Phase: This is the first phase, in which the two output nodes $\left\{O_{1}\right.$, Out $\left._{2}\right\}$ are shorted together by turning the reset transistor $\{\mathrm{M} 7\}$ ON. This is done to remove any previously latched states of the circuit, by bringing the two output nodes to near potentials. After which, the data in the magnetic tunnel junctions is accessed. This phase is similar to the pre-charge phase in any traditional memory sense amplifier.

As explained previously, the differential resistor configuration causes an imbalance between the pull-up and pull-down currents at the two output nodes. The current flowing in the larger resistance film will be smaller than the current flowing in the smaller resistance film. As a result, the pull-down currents differ from each other while the pull-up currents remain same in both legs, causing the difference current $(\Delta I)$ to flow through the reset switch to compensate the imbalance. The reset switch is turned on for sufficient time till the previous states are removed and the two output nodes settle at near potentials.

Latch Phase: This phase is started when the reset transistor is turned OFF, and $\{M 5, M 6\}$ then act as a high-gain positive feedback amplifier. Due to the positive feedback, the impedance looking into the source terminals of either M5 or M6 is a negative resistance, causing both the transistors to source a difference current ( $\Delta I$ ) through them. This difference current flows through the small equivalent capacitance at the drains of M5 and M6, giving rise to $\Delta V$ across the output nodes. The initial trajectory for the magnitude of the voltage difference between the drains of M5 and M6
is given approximately by

$$
\left|\frac{d \Delta V}{d t}\right|=\frac{2 \Delta I}{C_{d}}
$$

where $C_{d}$ is the total capacitance at the drain node of M5 or M6. This trajectory is followed for a short time, and then the resulting differential voltage at sense amplifier's outputs is rapidly amplified by the positive feedback present in the latch, driving Vout+ high and Vout - low for the case of positive $\Delta I$.

Figure 3.9 show the simulation results proving the proper working of this interface circuit. As can be seen from the figure, the SDT bits are flipped alternatively by the write01 signal and the output nodes $O u t_{1} \& O u t_{2}$ reflects this state correctly.

Transient Response
A


Figure 3.9 Simulation results of interface circuit-II

### 3.5.2.3 Design Considerations

There were a couple of design considerations that had to be taken care of:

- Selection of a PMOS reset switch: The maximum amount of current flowing through the magnetic tunneling junctions is $\sim 3 \mu A$. For minimum sized crosscoupled PMOS transistors, the amount of $V_{g s}$ needed to conduct $3 \mu A$ of $I_{d}$ is given as

$$
\begin{array}{r}
\frac{\mu_{p} C_{o x}}{2} \times \frac{W}{L} \times\left(v_{g s}-v_{t h}\right)^{2}=3 \mu A \\
\text { For }(\mathrm{W} / \mathrm{L})=1 \text { and } \mu_{p} C_{o x}=88 \mu A / v^{2} \\
\Rightarrow 44 \times 1 \times\left(v_{g s}-v_{t h}\right)^{2}=3 \\
\Rightarrow v_{g s} \approx 1 V \tag{3.2}
\end{array}
$$

Thus the two output nodes are around $(v d d-1 v)$. Given this condition, the amount of $V_{g s}$ available for the reset switch will be higher for a PMOS transistor $\left(v g s_{p} \sim v o u t-0\right)$ than a NMOS transistor $\left(v g s_{n} \sim v d d-v o u t\right)$. Since the reset switch has to bring both the output nodes to near potentials, it acts as a Pass transistor transmitting the voltage at the high output node to the low output node. Moreover a PMOS pass transistor is stronger in transmitting high voltage levels compared to a NMOS pass transistor which is stronger in transmitting low voltage levels [18]. Thus the reset switch was realized using a PMOS transistor.

- Choosing the PMOS reset switch $\{$ M7\} size: There are two conditions which have to be met, before we select the proper reset switch size:
- When the reset switch is open, the loop gain should be greater than unity $(T \gg 1)$ to start the positive feedback regeneration.
- When the reset switch is closed, loop gain has to be less than unity ( $T \ll 1$ ) to remove the previously latched state. If the loop gain is still greater than one, the positive feedback will be strong and thus will make the latched state

The reset switch acts a linear resistor between the two output nodes. If the resistance is high (i.e. small $\mathrm{W} / \mathrm{L}$ size) then we will have bigger $\Delta V_{\text {out }}$. This leads to one of the PMOS transistors being not knocked out from its Cut-off State and hence the previous latched state is not removed. If the resistance is small (i.e. big W/L size), the two output nodes are at nearly equal potentials. But then we will have a smaller $\Delta V_{\text {out }}$ and thus regeneration takes longer time. Hence we have to choose an appropriate $W / L$ size which is small but is sufficient enough to reduce the regeneration time. Several loop gain simulations were performed to verify the above concept before selecting the appropriate reset switch size.

- Layout Considerations: This interface circuit has the least area, since all the transistors are of minimum size width/length $(0.5 \mu / 0.5 \mu)$. Guard rings were added wherever possible to prevent latch-up formation and also to isolate the bias resistance from any digital switching noise. The layouts of this interface circuit along with the bit write circuitry is given in Appendix-A.


### 3.5.2.4 Merits \& Shortcomings

The main attractions of this kind of memory interface circuit are:

- It is much faster than the previous interface circuit, because of the positive regeneration available in the sense amplifier. And also due to the minimum sized PMOS transistors, capacitive loading on the output nodes was reduced.
- The output voltage swing obtained in this interface circuit is higher due to the latch operation. And this enabled us to use smaller sizes for the output buffers.

But there are certain limitations to the performance of this interface circuit:

- Static power dissipation is present when the interface circuit is active or in sense phase.
- It needs a separate reset phase and hence the control circuitry involved is higher.
- Mismatch in the NMOS transistors $\{$ M3, M4\} can cause an error in the output logic states. But due to the large resistance $(\approx 50 K \Omega-150 K \Omega)$ and magnetoresistance ( $\approx 20 \%-40 \%$ ) of the tunneling junctions, hopefully the mismatch effect in the threshold voltage should not affect the working of the interface circuit.


### 3.5.3 Interface Circuit-III

The complete schematic of this interface circuit is given in figure 3.10. Here too, schematics were designed for three ranges of magnetic resistance, as given in table 3.1.


Figure 3.10 Schematic of interface circuit-III

### 3.5.3.1 Structure

The design of this interface circuit is similar to interface circuit-II except that it employs cross coupled inverters and does not have a constant bias circuit. The first design requirement of restricting the voltage transients on the magnetic tunnel junctions is accomplished by using two shorting transistors $\{\mathrm{M} 8, \mathrm{M} 9\}$. These transistors are heavily biased in the linear region and provide a low impedance path from the sources of $\{\mathrm{M} 3, \mathrm{M} 4\}$ to ground. Hence most of the inverter "short-circuit" [18] current passes
through them and reduces the voltage drop across their drains ( $V_{d s}$ ). And since $V_{d s}$ of these transistors decides the voltage drop across the tunnel junctions, we can restrict both the current and voltage transients across the tunnel junctions.

The second design requirement of current logic state sensing is done using the cross coupled inverters. These inverters form a positive feedback amplifier able to regenerate the current difference between the two legs into full logic levels. The configuration is similar to interface circuit II, wherein we have a combination of differential current mode sense amplifier and a latch. Detailed explanation of the working principles will be explained in later sections. The cross coupled inverters are formed from the transistors $\{(\mathrm{M} 3, \mathrm{M} 5),(\mathrm{M} 4, \mathrm{M} 6)\}$.

Here too we use a reset switch formed out of NMOS transistor $\{\mathrm{M} 7\}$. This helps in the correct regeneration of the output logic and comes into action in the first phase of sensing.

### 3.5.3.2 Functionality

Similar to interface circuit II, we have two phases in the sensing procedure.
Reset Phase: In this phase, the reset switch $\{M 7\}$ is turned ON and the two outputs $\left\{\right.$ Out $\left._{1}, O u t_{2}\right\}$ are brought to near potentials. Due to the differential topology, there will be a current imbalance between the two legs. This difference current would then flow through the reset switch to compensate for the current imbalance. Note that the shorting transistors are always ON , and hence most of the current will be flowing through them. Hence the voltage across the tunnel junctions is restricted but is sufficient enough to generate substantial current difference in the legs.

Latch Phase: This phase is started when the reset switch M7 is turned OFF and the two inverters come into positive feedback configuration. Due to the positive feedback, the small amount of initial current difference will start the regeneration and cause the outputs to reach correct logic levels. All these while, the shorting transistors present a low impedance path to the inverters and aid in restricting the current through the tunnel junctions.


Figure 3.11 Simulation results of interface circuit-III

Figure 3.11 show the simulation results proving the proper working of this interface circuit. As can be seen from the figure, the SDT bits are flipped alternatively by the write01 signal and the output nodes $O u t_{1} \& O u t_{2}$ reflects this state correctly.

### 3.5.3.3 Design Considerations

There were a couple of design considerations that had to be taken care of:

- Selection of a reset switch size: As explained previously, the reset switch is needed to remove any previously latched state. And for that to happen, the loop gain of the circuit should be less than 1 when the reset switch is ON. Hence numerous loop gain simulations were performed, to verify the above requirement and also the
correct circuit functionality. An appropriate reset switch size was chosen which had maximum $\Delta V_{\text {out }}$ and gave the least regeneration time.
- Separate enable signals for $\{$ M1, M2 $\}$ : These transistors are the read/write enable transistors, used for either connecting or disconnecting the tunnel junctions from the interface circuit. Previously, we used the same "Rwen" signal to control both the write circuitry and the enable transistors. But in this interface circuit, a separate signal had to be used for these transistors in order to reduce the voltage transients across the tunnel junctions. The relation between the new RWen 1 and $R W$ en signals is given below in figure 3.12. As shown these transistors are turned off prior to start of writing phase and turned on later than the end of writing phase. This way, the transients introduced by parasitic capacitance of these transistors is reduced. The layouts of this interface circuit along with the bit write circuitry is given in Appendix-A.


Figure 3.12 Relation between the RWen and RWen1 signals

### 3.5.3.4 Merits \& Shortcomings

The main attractions of this kind of menory interface circuit are:

- No Static Power dissipation is present in this circuit. Hence it consumes much lesser power compared to the other two interface circuits.
- It is much faster compared to the other two interface circuits, due to the presence of cross-coupled inverters. The initial differential current gain obtained from this cross-coupled inverter configuration is much higher compared to the cross-coupled PMOS transistors in interface circuit II.
- No Additional Bias circuit needed. Hence even though we have more number of transistors in this interface circuit, the overall area is much less compared to the previous two interface circuits. This reduction is due to the absence of the huge poly bias resistor. Hence it is a favorable solution to memory sense-circuitry's penalty in case of high density MRAMs.
- Full range of output voltage swing is obtained in this interface circuit due to the actual latch operation. And this enabled us to use smaller sizes for the output buffers.
- An interesting variation of this circuit, is to use this as a modified 6T SRAM cell that may be read and written as a conventional CMOS memory cell. But at the same time, also contains SDT shadow memory that may be read at any time by engaging the shorting transistor.

But there are certain limitations to the performance of this interface circuit:

- Circuit sensitivity to Mismatch is higher and hence probability of failure is quite substantial. Mismatch in these shorting transistors may cause degradation in the amount of differential current available from the circuit and may even cause failure of the magnetic bits, in case the voltage transients exceed the maximum tolerance. Hence care must be taken to reduce the mismatch effects from these shorting transistors.


### 3.5.4 Interface Circuit-IV

These interface circuits are variants of the first two interface circuits. Figure 3.13 and figure 3.14 give the complete schematic of the two types of interface circuit IV.


Figure 3.13 Schematic of interface circuit-IV - case 1

As seen in these figures, the only variation in this interface circuit design as compared to their alternates is in the bias configuration. Here we use true replica biasing scheme by employing magnetic tunnel junctions as the bias resistor.

### 3.5.4.1 Structure

The structure of these interface circuits is identical to the first two interface circuits, except for variations in the bias scheme used. The bias string is realized by using magnetic tunnel junctions in place of poly resistors. Hence true replica biasing scheme is realized, since the bias leg is an exact replica of the NMOS path in the sense amplifier. The reason behind such scheme is to replicate the variations of the magnetic memory bits in the bias resistor too. By doing so, if we can restrict the voltage on the magnetic bias resistor under all conditions, we will be able to restrict the voltage transients on the memory bits as well. Thus the bias string can follow the process variations induced in the memory bits and ensure correct operation of the bits.

However, a problem with this biasing scheme is to decide the value of the bias resistor. One possible solution is to choose an average of the two differential magnetic resistors. But in our scheme, we fixed the bias resistor to be equal to either of the differential


Figure 3.14 Schematic of interface circuit-IV - case 2
resistor value, still able to restrict the voltage transients on the actual memory resistor bits. And also we can write the bias resistor into either of the differential state using its dedicated bit write circuitry. Thus, we can realize the bias resistor as either HIGH or LOW resistance, and thereby control the voltage transients on the magnetic bits.

The rest of the circuitry consisting of sense amplifier and output stages is identical to their alternatives. Refer to sections 3.5.1.1 and 3.5.2.1 for the detailed explanation.

### 3.5.4.2 Functionality

The working principles of these interface circuits are identical to the first two interface circuits, the details of which can be read in those respective sections. One key aspect of this interface circuit is its provision for two different biasing schemes. Figure 3.15 shows the two types of bias connections available in this circuit. Three separate pads \{latch_bias, Ibias, BiasR\} are added to the bias network, which enable us to use an external amplifier to realize a gain boosted structure or connect the NMOS transistor M8 in the traditional diode connected configuration.

The advantage of a gain-boosted structure is that it helps in precisely controlling the voltage transients across the magnetic differential resistors and keeps them under a


Figure 3.15 The different bias configurations in interface circuit-IV
known reference voltage. This is possible due to the negative feedback and the high open loop gain of external amplifier. In such a configuration the BiasR node voltage gets fixed almost near to Vref. And that voltage is maintained at the same level, by controlling the gate voltage of M8 to take care of any variation in the circuit conditions. Hence if we can provide an external stable bias voltage Vref lesser than the maximum allowable voltage drop across the magnetic tunnel junction, then the design requirement of restricting the voltage transients on the magnetic bits is guaranteed under all circuit conditions. The external amplifier can typically be realized using high gain IC741 op-amps. Figure 3.15 shows such a connection using IC741 op-amp part. Note that the $V_{g s}$ drop of $\{$ M8\} fixes the bias current and hence a resistor is used for connecting the drain of $\{\mathrm{M} 8\}$ to Vdd.

Also a special enable signal BIAS_EN is used for controlling the $\{\mathrm{M} 9\}$ switch, to disconnect the bias network while writing the bias resistor. A bit write circuitry is dedicated for the bias magnetic resistor, to be able to write into either HIGH or LOW resistance states. This way, we can control the voltage transients across the two differential magnetic bits appropriately.

There are no special design requirements for these interface circuits apart from those mentioned in the first two interface circuit sections. Apart from its main attraction of
gain boosted structure there are no added advantages. Care must be taken to prevent any possible pad induced oscillations. Moreover we need more write circuitry involved in this interface circuit, making it less favorable under density criterion. Refer to Appendix-A for the layouts of these circuits.

## 4 MISMATCH AND DESIGN CONSIDERATIONS

Mismatch plays a significant role in determining the proper functionality of the designed interface circuits. It degrades the available input signal for sense amplifiers and might even cause the failure of interface circuits. Hence care must be taken during the design phase by accounting for a finite mismatch. There are two principal sources of mismatch in our designs - the differential resistor pair and the MOSFETs. The following sections would give the complete details of these two mismatch sources and how they affect the functionality of our designed interface circuits.

### 4.1 SDT Resistor Mismatch

When there is a resistance mismatch, the resistance difference produced by a pair of differential films is enhanced in one state and degraded in other. If a perfect sensing amplifier is provided, then the available resistance mismatch should be smaller than the maximum resistance change in order for the interface circuits to function correctly. Moreover this also indirectly affects the speed of the interface circuit, since the obtained differential resistance determines the available input signal level for the sense amplifier. Such a mismatch effect can be lumped into the SDT ratio formula [19] and will reflect as a reduction in the effective SDT ratio.

The new nominal resistance of the differential pair is defined as the average resistance of the two-mismatched resistors, $R_{1}$ and $R_{2}$. at the nominal condition as given in equation (4.1). The resistance difference is the minimum difference produced between the two resistors and equation (4.2) gives us the worst case condition. The effective SDT ratio is then given in equation (4.3), as the ratio of the change in resistance to the effective
nominal resistance. As seen from the equation, any amount of mismatch reduces the effective magneto-resistivity obtained.

$$
\begin{align*}
& R_{\text {Neff }}=\frac{R_{N 1}+R_{N 2}}{2}  \tag{4.1}\\
& \Delta R_{\text {eff }}=M I N\left\{R_{1}, R_{2}\right\}_{\text {@high_resistance_state }}-M A X\left\{R_{1}, R_{2}\right\}_{\text {@low_resistance_state }}  \tag{4.2}\\
& \text { Effective Ratio of resistance change }=\frac{\Delta R_{\text {eff }}}{R_{\text {Neff }}} \tag{4.3}
\end{align*}
$$

The sensitivity to $\Delta R$ of the interface circuits is high due to the other mismatches present in their designs. Hence a minimum amount of SDT ratio is needed for the interface circuits to work properly. And thus, from the above equations, a considerable reduction in the effective SDT ratio might even lead to the failure of the interface circuits.

### 4.2 Transistor Mismatch

The principal mismatch contributing factors in a MOSFET can be grouped into two main categories - threshold voltage mismatch $\left(V_{t h}\right)$ and transconductance $(\beta)$ mismatch. Even though the sources of these mismatches are different, they more or less follow the same trend. A lot of research had been done in the past [20, 21, 22], and well characterized equations have been formulated for describing such statistical variations. Equations (4.4, 4.5) show the model for characterizing a parameter's mismatch through its standard deviation.

$$
\begin{align*}
\sigma_{\Delta V_{t}} & =\frac{A_{\Delta V_{t}}}{\sqrt{W L}}+S_{V_{t}} D  \tag{4.4}\\
\sigma_{\Delta \beta / \beta} & =\frac{A_{\Delta \beta / \beta}}{\sqrt{W L}}+S_{\Delta \beta / \beta} D \tag{4.5}
\end{align*}
$$

where $W$ and $L$ are transistor's width and length, and $D$ is the distance between two such identical transistors. The two terms in the equation denote the two distinct physical causes of a parameter's mismatch. The $S_{D}$ term denotes a systematic deviation in the parameter's value, caused due to known gradients present on a wafer. Since it is dependent on the wafer gradients, such mismatch effects are proportional to the distance between the two mismatched transistors. But such gradients can be compensated by
special layout techniques like inter-digitation and common centroid layouts. And also the advancements in present day wafer technologies have reduced the amount of gradients present. Hence, such mismatches would be negligible for transistors placed at near distances and thus will be neglected in further analysis.

Random mismatch, on the other hand, is caused due to noise like perturbations in the device's parameters along a die. These mismatches due to their random nature, cannot be reduced by any standard techniques, and should not be neglected. As shown in the equations, the amount of mismatch produced in a transistor pair is less for larger area transistors. Therefore a design trade off arises for choosing the appropriate size of our MOSFETs in interface circuits, which yield comparable performance with tolerable mismatch.

The matching of each transistor pair is very critical since the circuits have been designed to process small input signals. A slight amount of variation can lead the circuits to latch into wrong state. To help understand the impact of transistor mismatch, the functional behavior of all interface circuits are investigated under mismatcl conditions

### 4.2.1 Interface Circuit-I

The main sources of error in this circuit are the mismatches in bias transistors, M3 and M4. Both types of transistor mismatches - threshold voltage ( $\sigma_{\Delta V_{t h}}$ ) and transconductance ( $\sigma_{\Delta \beta / \beta}$ ) can have an significant affect on latch functionality. But apparently threshold voltage mismatch plays a dominant role and hence will be considered first.

Figure 4.1 shows the interface circuit's pull down path under normal operating conditions. The pull down path's purpose is to introduce an initial current imbalance ( $\Delta I_{N}$ ), which can then be amplified by the high-gain PMOS current mirror. Ideally, the initial current imbalance ( $\Delta I_{N}$ ) introduced is determined solely by SDT's differential resistance. But under the presence of threshold voltage mismatch, this differential current signal can be reduced and might even reverse its direction causing the circuit to latch into wrong state. Equation (4.7) gives the condition when the latch starts to fail. $\Delta V_{T_{N}}$ represents the threshold voltage difference between the two bias transistors. As indicated
in the equation, the latch will fail when the initial current difference $\left(\Delta I_{N}\right)$ is zero even under the presence of a finite differential SDT resistance. This is caused by the equal excess voltages $\left(V_{d}^{\text {sat }}\right.$ ) of the two bias transistors even when their gate voltages $\left(V_{g s}\right)$ are different, as shown in equation (4.6). Since MOSFET's saturation current ( $I_{d}^{\text {sat }}$ ) is determined by its excess voltage, the two bias transistors conduct equal current even when there is a finite SDT resistor difference.

$$
\begin{align*}
V_{g s_{3}} \neq V_{g s_{4}}, \text { but } V_{g s_{3}}-V_{T_{N_{3}}} & =V_{g s_{4}}-V_{T_{N_{4}}} \\
\Rightarrow \Delta V_{T_{N}} & =V_{g s_{3}}-V_{g s_{4}} ; \text { if } V_{T_{N_{3}}} \geq V_{T_{N_{4}}}  \tag{4.6}\\
I_{R_{1}}=I_{R_{2}}=I_{N} \text { and } V_{b i a s} & =I_{N} R_{1}+V_{g s_{3}}=I_{N} R_{2}+V_{g s_{4}} \\
\Rightarrow V_{g s_{3}}-V_{g s_{4}} & =I_{N}\left(R_{2}-R_{1}\right)=I_{N}\left(\Delta R_{N}\right) \\
\Rightarrow \Delta V_{T_{N}} & =I_{N}\left(\Delta R_{N}\right)(\text { from eqn4.6 }) \tag{4.7}
\end{align*}
$$

Note that, in both equations, currents through the SDT resistors are replaced by an equal nominal current $I_{N}$. Equation (4.7) also gives an estimate of the minimum nominal latch current $I_{N}$, for a given threshold voltage mismatch $\left(\Delta V_{T_{N}}\right)$ and a given SDT magnetoresistance $\left(\Delta R_{N}\right)$. Choosing a bias current greater than this minimum value $\left(I_{N}\right)$, helps the input signal ( $I_{N} \cdot \Delta R_{N}$ ) to overcome the threshold mismatch ( $\Delta V_{T_{N}}$ ). Hence by considering a finite mismatch during the design phase, helps us choose proper bias conditions for ensuring the correct functionality of our interface circuit.

To verify the above theory, simulations were done with threshold voltage mismatch introduced between the two bias transistors. Figure 4.2 shows the method in which a dc voltage source is put in series with one of the transistor's gate, thereby simulating a mismatch in threshold voltages.

From the given design parameters, wherein $I_{N}=3 \mu A$ and $R_{N}=25 K \Omega$, we get the maximum threshold voltage mismatch for a MR of $20 \%$ to be equal to, $\Delta V_{T_{N}}=$ $I_{N} \times \Delta R_{N}=3 \mu A \times(0.2 \times 25 K \Omega)=15 \mathrm{mv}$. The interface circuit should function properly as long as the dc voltage value introduced between the gates is less than 15 mv . Figure 4.3 shows the simulation results for a threshold voltage mismatch of 15 mv , which proves the fact that interface circuit-I can work even with $15 m v$ mismatch. And Figure


Figure 4.1 NMOS bias path under normal operating conditions
4.4 proves that $15 m v$ is the maximum threshold voltage mismatch that interface circuit-I can handle - as the simulations fail for a value of 20 mv .

Similarly, if we have a transconductance factor mismatch, the interface circuit will fail if the two pull down currents are identical even when there is a SDT resistance difference. Thus, this mismatch creates a similar condition of offsetting the initial current difference introduced by the differential resistors. Modeling the two bias transistors's transconductance factors as $\left(\beta_{N n}+\Delta \beta_{n} / 2\right)$ and ( $\beta_{N n}-\Delta \beta_{n} / 2$ ), equation (4.8) [19] shows the maximum tolerable mismatch allowed for this interface circuit to function correctly. Similar to the threshold voltage mismatch equation shown previously (equation 4.7), $\Delta \beta_{n}$ is linearly proportional to the input resistance. Besides that, $\Delta \beta_{n}$ is also linearly proportional to the $V_{\text {bias }}$ of the transistors. As a result, larger input resistance and biasing voltage can reduce the effect of the transconductance factor mismatch.

$$
\begin{align*}
\left(\beta_{N}+\frac{\Delta \beta_{n}}{2}\right)\left(V_{g s_{3}}-V_{T_{3}}\right)^{2} & =\left(\beta_{N}-\frac{\Delta \beta_{n}}{2}\right)\left(V_{g s_{4}}-V_{T_{4}}\right)^{2} \\
\frac{\Delta \beta_{n}}{\beta_{N}} & \approx \frac{2 I_{N} \Delta R_{N}}{\left(V_{\text {bias }}-V_{T}-I_{N} R_{N}\right)} \\
& =\beta_{N}\left(V_{\text {bias }}-I_{N} R_{N}-V_{T_{N}}\right) \Delta R \tag{4.8}
\end{align*}
$$

The top PMOS current mirror transistors may also have some mismatch and might affect the working of interface circuit. But these transistors had been designed with


Figure 4.2 Method for simulating threshold voltage mismatch
large gate lengths. And according to equations (4.4) and (4.5) transistors with larger effective areas tend to show lesser mismatch effects. Therefore, the mismatch effects of these two transistors are neglected from our analysis.

### 4.2.2 Interface Circuit-II

The mismatch effects of this interface circuit can be studied by observing the amount of error current introduced in the reset switch path. Ideally, the differential SDT resistance creates a current imbalance in the circuit, which then flows through the reset switch during precharge phase. But under the presence of any mismatch, there can be a undesirable error current introduced in the same reset path to upset the signal current $(\Delta I)$. The interface circuit will function correctly until a point where this error current starts to dominate the signal current leading to functional failure.

The mismatch error current can be produced both by the NMOS bias transistors and the cross-coupled PMOS transistors. First let us consider the pull-down NMOS bias path. Since this part of the circuit is similar to the bias path in interface circuit I, the same analysis of the previous section can be applied here too. Figure 4.5 shows the pull down section of the interface circuit during the precharge phase. The dotted line in the figure represents the connection introduced by the reset switch. As shown in


Figure 4.3 Simulation results of interface circuit-I for $\Delta V_{t h}=15 \mathrm{mv}$
the figure, the mismatches in bias transistors can be represented by an equivalent error current ( $\Delta I_{n}$ ) flowing opposite to the signal current $(\Delta I)$. The circuit will start to fail when this error current equals the signal current, thus causing both pull down currents to be equal even under a presence of finite SDT resistance. At this point, the circuit gets locked into a meta-stable state. The same equations as (4.7, 4.8) is applicable for this analysis too, to quantify the maximum tolerable amount of threshold voltage mismatch and transconductance mismatch in the NMOS bias transistors.

Figure 4.6 shows the pull up path along with the PMOS transistor mismatches. Similar to the pull down path, the mismatches in the PMOS cross-coupled transistors can be represented by an equivalent error current $\Delta I_{p}$ in the reset switch path. Again, the circuit is in precharge phase and the dotted line represents the reset switch connection. Ideally, the pull-up paths conduct a nominal current $I_{N}$ while the pull-down paths have a current imbalance caused due to resistor difference. When the reset switch is turned


Figure 4.4 Simulation results of interface circuit-I for $\Delta V_{t h}=20 \mathrm{mv}$
off, due to this imbalance between pull-up and pull-down paths, an initial potential difference develops across the output nodes. And this difference will eventually trigger the signal regeneration and complete the read cycle. But under the presence of any mismatch, the error current might dominate the signal current, causing the circuit to latch into either a meta-stable state or even worse a wrong logic state.

When only threshold voltage mismatch is taken into account, $\Delta I_{p}$ can be determined with equation (4.9) [19]. The two thresholds voltages are denoted as $\left(V_{T p}+\Delta V_{T_{P}} / 2\right)$ and ( $V_{T p}-\Delta V_{T_{P}} / 2$ ). Equation(4.10) [19] shows the corresponding tolerable threshold voltage mismatch in these two PMOS transistors. Also, if transconductance factor mismatch is considered, then equations (4.11) and (4.12) [19] show the respective relationships


Figure 4.5 Mismatch currents in the NMOS bias path
between $\Delta I_{p}$ and $\Delta \beta_{p}$.

$$
\begin{align*}
\Delta I_{p} & =\frac{I_{1}-I_{2}}{2} \\
& =\frac{\beta_{p}}{2} \times\left(V d d-V_{\text {out }}-V_{T p}\right)\left(\Delta V_{T p}\right)  \tag{4.9}\\
\Delta V_{T p} & =\frac{2 \Delta I_{p}}{\beta_{p}\left(V d d-\text { Vout }-V_{T p}\right)}  \tag{4.10}\\
\Delta I_{p} & =\frac{\Delta \beta_{p}}{2}\left(V d d-\text { Vout }-V_{T p}\right)^{2}  \tag{4.11}\\
\frac{\Delta \beta_{p}}{\beta_{p}} & =\frac{\Delta I_{p}}{I_{N}} \tag{4.12}
\end{align*}
$$

Lumping all the error terms together, we get an equivalent error current, $\Delta I_{n}+\Delta I_{p}$, flowing through the reset switch. To have the interface circuit function correctly, the $\Delta I$ term must be greater than the error current, $\Delta I_{n}+\Delta I_{p}$, to have the necessary direction of current flow in the reset switch. Hence the designer should be aware of this situation, and should carefully budget the signal current, $\Delta I$, to overcome the mismatch currents. For some cases, larger nominal operating current, $I_{N}$, or larger nominal resistor, $R_{N}$, might be needed to enhance $\Delta I$. Larger transistors might be needed as well to reduce the error current, $\Delta I_{n}+\Delta I_{p}$, in order to make the circuit function correctly. Simulations similar to


Figure 4.6 Mismatch currents in the PMOS cross-coupled path
interface circuit-I analysis were performed, by simulating the circuit's mismatch effects through DC voltage sources placed in series with respective transistor pair gates.

### 4.2.3 Interface Circuit-III

The mismatch analysis of this interface circuit is very similar to the previous two sections, except for the NMOS pull down path. This interface circuit consists of two cross-coupled inverters and the pull-up PMOS connections are same as the interface circuit II. Hence the mismatch characterizing equations of $(4.9,4.10,4.11,4.12)$ can be applied for this case. The NMOS pull down path consists of two cross-coupled NMOS transistors and their main function is to introduce a current imbalance during the precharge phase. The mismatch analysis of these transistors can be done on similar lines of cross-coupled PMOS transistors. Thus, the circuit will fail due to these transistor's mismatches, if the two pull down currents are equal even under the presence of a finite SDT resistor difference. Equation (4.13) show the maximum tolerable threshold voltage mismatch of pull-down NMOS transistors. And equation (4.14) shows a similar
relationship for the transconductance mismatch factor.

$$
\begin{align*}
\Delta V_{T_{N}} & =V_{T_{4}}-V_{T_{3}}=I_{N} \cdot \Delta R  \tag{4.13}\\
\frac{\Delta \beta_{n}}{\beta_{N}} & \approx \frac{2 I_{N} \Delta R_{N}}{\left(V_{\text {out }}-V_{T}-I_{N} R_{N}\right)} \\
& =\beta_{N}\left(V_{\text {out }}-I_{N} R_{N}-V_{T_{N}}\right) \Delta R \tag{4.14}
\end{align*}
$$

But apart from the above two mismatch sources, this interface circuit also suffers due to the mismatches in shorting transistors M8 and M9 (refer to figure 4.7). Ideally, the shorting transistors provide a low impedance path to ground for the inverter's saturation current. During precharge phase, the nominal current $\left(I_{N}\right)$ of this circuit is quite high $\sim 16 \mu A$. Therefore shorting transistors were designed to take almost $\sim 90 \%$ of the nominal current $\left(I_{N}\right)$, while the rest $10 \%$ flows through the SDT resistors. Since current through the SDT resistors is reduced, we could restrict the voltage drop across the tunnel junctions below the specified limit. If there is no mismatch between the shorting transistors, the only difference in resistance is due to tunnel junctions and the same amount of $\Delta I$ is obtained with or without shorting transistors. Thus the interface circuit works well with considerable increase in response speed. But when mismatch is present between the shorting transistors, they themselves exhibit a difference in their linear region resistance $\left(g_{d s}\right)$. Due to this difference, an additional input differential current is created apart from that caused by the SDT differential resistors. This mismatch current can either aid or degrade the actual input signal; and hence might even lead to functional failure. The circuit will start to fail, when the two pull down currents are made equal even under the presence of a finite differential SDT resistance. This condition can be quantified and is shown in equation 4.15 where we use conductances.

$$
\begin{align*}
\text { under mismatch, }\left(I_{N}\right)\left(R_{1} \| \frac{1}{g_{d s_{8}}}\right) & =\left(I_{N}\right)\left(R_{2} \| \frac{1}{g_{d s_{9}}}\right) \\
\Rightarrow \frac{1}{R_{1}}+g_{d s_{8}} & =\frac{1}{R_{2}}+g_{d s_{9}} \\
\text { if } R_{1}<R_{2} . \text { then } \Rightarrow \Delta g_{S D T_{12}} & =-g_{d s_{89}} \tag{4.15}
\end{align*}
$$



Figure 4.7 Mismatch effects in the shorting transistors

Correlating the linear conductance $\left(g_{d s}\right)$ of shorting transistor to its threshold voltage and transconductance factors, we can derive a relationship for the maximum tolerable mismatch in these transistors. Equation 4.16 shows the maximum tolerable threshold voltage mismatch and is found to be inversely proportional to the nominal SDT resistance. Therefore, if we have a lower nominal resistance or a higher magnetoresistance $\left(\Delta R_{N}\right)$ we can have a larger error margin for threshold mismatches. Or in other words, this interface circuit is less sensitive to threshold voltage mismatches for lower nominal SDT resistances. Equation 4.17 shows a similar relationship for transconductance factor mismatch. It is also inversely proportional to SDT nominal resistance and nominal current. Thus such mismatches can be reduced by choosing lower nominal SDT resistances or lower nominal currents $\left(I_{N}\right)$.

$$
\text { since in linear region, } \begin{align*}
& g_{d s}=\beta\left(V_{g s}-V_{t}-V_{d s}\right) \\
& \text { also, } g_{S D T_{12}} \approx \frac{\Delta R_{N}}{R_{N}^{2}} \\
& \Rightarrow \Delta g_{S D T_{12}}=\beta \cdot \Delta V_{T_{N}} \\
& \Rightarrow \Delta V_{T_{N}} \approx \frac{1}{\beta} \cdot \frac{\Delta R_{N}}{R_{N}^{2}}  \tag{4.16}\\
& \text { similarly, } \begin{aligned}
\Delta g_{S D T_{12}} & =\Delta \beta_{N}\left(V_{g s}-V_{T_{N}}-V_{d s}\right) \\
\Rightarrow \frac{\Delta \beta_{N}}{\beta_{N}} & \approx \frac{1}{I_{N}} \cdot \frac{\Delta R_{N}}{R_{N}^{2}}
\end{aligned},=\text {. }
\end{align*}
$$

Thus considering all factors, this interface circuit works well with lower ranges of nominal SDT resistances. Care must be taken to reduce the nominal current ( $I_{N}$ ) or increase the W/L ratio of shorting transistors to reduce the mismatch effects in this design.

### 4.3 Mismatch Characterization

All the analysis till now assumed that the designer has a knowledge of the possible threshold voltage and transconductance factor mismatches for the various transistor sizes used in these designs. But such data was not available for TSMC $0.35 \mu$ process in the literature and hence separate characterization dies had to be designed for this purpose. Layout of the 4 dies used for characterizing the transistor mismatches is shown in Appendix-A.

A simple method of characterizing the mismatch between two identical transistors is to use a differential pair. Figure 4.8 shows a simple differential pair with a common source terminal and whose gates are separated by a distance 'd' on the wafer. When equal gate voltages $\left(V_{g s}\right)$ are applied, the difference in their drain currents indicates the amount of mismatch present. As seen from the die layouts in Appendix-A, these characterization dies waste considerable amount of precious silicon. Moreover these designs are pad limited; meaning we could accommodate only those many transistors as we can provide pads for. Since these dies had 20 pads, we could accommodate only 5 differential pairs. Under these constraints, we had to get the maximum possible mismatch data for the transistor sizes used in our interface circuits.

Hence two cases of mismatch characterization were considered for the both PMOS and NMOS transistor types:

- Mismatch as a function of Transistor size: In this case, 5 different transistor sizes were realized. The sizes were varied from the minimum size of $0.4 \mu / 0.35 \mu$ upto $6.4 \mu / 0.35 \mu$, periodically increasing the size by twice each time. The distance between the gates was maintained constant, and hence this design will help us find the constants $A_{\Delta V_{t}}$ and $A_{\Delta \beta / \beta}$ in equations (4.1, 4.2). Figure A. 1 shows a typical


Figure 4.8 A simple differential pair used to characterize mismatch
layout for this case. Note that the distance between the gates is maintained the same while the transistor size was varied.

- Mismatch as a function of gate separation distance: In this case, only the distance between the transistor gates is varied while transistor size was kept constant. A minimum size of $0.4 \mu / 0.35 \mu$ was used for all the transistors. The distance was varied both in the X and Y directions, in order to study the gradient effects along both die axes. This case will help us find the $S_{D}$ constants in equations (4.1, 4.2). Figure A. 2 shows the typical layout for this case.

The mismatch results are obtained using HP4145A semiconductor parameter analyzer and Cascade Alessi REL-4800 analytical probe station. The results obtained and conclusions drawn will be explained in detail in the next chapter.

### 4.4 Design Considerations and Procedures

In this section, we will be describing a procedure to design these interface circuits for a particular yield specifications, under a given process mismatch data. Since yield requirements are specified, the most important design parameter would be the various mismatches present in the circuit. And as shown in the previous analysis, transistor mismatches plays a significant role in determining the correct functionality of interface circuits. Since we do not have the transistor sizes to start with, this procedure would
be an iterative process and the specified design steps will be revisited until we meet all specifications and functionality.

Interface circuit-I is considered for this analysis, but similar methods can be derived for the other interface circuits too. A mathematical treatment is given along with this procedure, and also $M A T L A B^{T M}$ implementation is done for automating the same.

The first step in the design procedure will be to fix the DC operating conditions $\wedge^{f} \sim$ interface circuit. It is assumed that the nominal SDT resistance and magnetoresistance values have been provided. The DC operating conditions are usually fixed by the maximum voltage that can be sustained across SDT resistors and by the number of SDT resistors connected in series for signal enhancement. Hence for a given ' $k$ ' number of SDT resistors in series, and a maximum bias voltage of $V_{b}$ across a single SDT resistor, equation 4.18 gives the maximum current allowable through the circuit.

$$
\begin{equation*}
I_{N}=k \times \frac{V_{b}}{2 R_{N}+\Delta R_{N}} \quad ; \text { where } R_{N} \text { is Nominal SDT resistance } \tag{4.18}
\end{equation*}
$$

The nominal operating current has to be less than this value under all conditions and process corners. After the DC operating current is selected, the SDT resistance mismatch should be taken into account. When there is mismatch in the resistor pair, the effective change in resistance will be degraded and the generated input signal $(\Delta I)$ will be reduced. Considering worst case variations in the differential SDT resistance, equation 4.19 gives us the minimum signal produced.

$$
\begin{equation*}
\left|\Delta I_{\text {signal }_{\min }}\right|=\left|\frac{\partial I}{\partial R} \cdot \Delta R\right|=\frac{2 I^{2} \Delta R}{V_{b}+I R-V_{t}} \tag{4.19}
\end{equation*}
$$

Now in order to satisfy the yield requirements, this minimum signal should be ' $m$ ' sigmas greater than the error current present in the circuit. Hence knowing the minimum signal produced in the circuit, gives us the maximum error current allowable. Figure 4.9 shows this condition assuming a normal probability distribution for the error current.

Given this condition, we can split the error current among the NMOS and PMOS transistors, in order to calculate their corresponding variances. Equations 4.20 and 4.21 show the respective error current variances, where $m_{\text {split }}$ refers to the distribution of total error current among PMOS and NMOS paths. Given these mismatches and drain


Figure 4.9 Required relation between the minimum signal current produced and maximum error current present
current equations for individual transistors, we can then solve for the optimum transistor sizes which satisfy yield requirements and also provide good functionality specs.

$$
\begin{align*}
\sigma_{N M O S} & =m_{\text {split }}\left[\frac{1}{m} \Delta I_{\text {sig }}-\sigma_{\text {noise }, S D T}\right]  \tag{4.20}\\
\sigma_{P M O S} & =\left(1-m_{\text {split }}\right)\left[\frac{1}{m} \Delta I_{\text {sig }}-\sigma_{\text {noise }, S D T}\right] \tag{4.21}
\end{align*}
$$

The following steps will give a more detailed mathematical proof of the solution. The total signal current obtained in the interface circuit would be a function of many parameters which can be grouped as

Total Signal current, $\Delta I_{N}=f\left(\Delta R, \Delta V_{t}, \Delta \beta\right)$
where, Actual signal current, $\Delta I=\frac{\partial I}{\partial R} \Delta R$
Error current from NMOS path, $\Delta I_{n}=\frac{\partial I}{\partial V_{t}} \Delta V_{t_{n}}+\frac{\partial I}{\partial \beta} \Delta \beta_{n}$
Error current from PMOS path, $\Delta I_{p}=\frac{\partial I}{\partial V_{t}} \Delta V_{t_{p}}+\frac{\partial I}{\partial \beta} \Delta \beta_{p}$

Under nominal operating conditions, $I_{N M O S}=I_{P M O S}$

$$
\text { where, } \begin{align*}
I_{N M O S} & =I=\frac{\beta_{n}}{2}\left(V_{\text {bias }}-I R-V_{t_{n}}\right)^{2} \\
I_{P M O S} & =I=\frac{\beta_{p}}{2}\left(V_{\text {bias }}-I R-V_{t_{p}}\right)^{2} \tag{4.25}
\end{align*}
$$

And, $\Delta I_{\text {actual }}=\left(\frac{\partial I}{\partial R} \cdot \Delta R\right)+\left[\left(\frac{\partial I}{\partial V_{t}} \cdot \Delta V_{t_{n}}\right)+\left(\frac{\partial I}{\partial \beta} \cdot \Delta \beta_{n}\right)\right]+(\ldots$ contd $\ldots)$

$$
\begin{equation*}
(\ldots \text { contd... })\left[\left(\frac{\partial I}{\partial V_{t}} \cdot \Delta V_{t_{p}}\right)+\left(\frac{\partial I}{\partial \beta} \cdot \Delta \beta_{p}\right)\right]+\Sigma I_{N o i s e} \tag{4.26}
\end{equation*}
$$

$$
\begin{align*}
& \text { Now, } I=\frac{\beta_{n}}{2}\left(V_{\text {bias }}-I R-V_{t_{n}}\right)^{2} \\
\Rightarrow \quad & \frac{\partial I}{\partial R}=2 \times \frac{\beta_{n}}{2}\left(V_{\text {bias }}-I R-V_{t_{n}}\right)\left(-I-R \frac{\partial I}{\partial R}\right)=\frac{2 I}{V_{\text {bias }}-I R-V_{t_{n}}}\left(-I-R \frac{\partial I}{\partial R}\right) \\
\Rightarrow \quad & \frac{\partial I}{\partial R}\left[1+\frac{2 I R}{V_{b}-I R-V_{t_{n}}}\right]=\frac{-2 I^{2}}{V_{b}-I R-V_{t_{n}}} \quad\left[V_{\text {bias }}=V_{b}\right] \\
\Rightarrow \quad & \frac{\partial I}{\partial R}=\frac{-2 I^{2}}{V_{b}+I R-V_{t_{n}}}\left[V_{\text {bias }}=V_{b}\right]  \tag{4.27}\\
\Rightarrow \quad & \text { Sensitivity, } S_{R}^{I}=\frac{R}{I} \frac{\partial I}{\partial R}=\frac{-2 I R}{V_{b}+I R-V_{t_{n}}} \quad\left[V_{\text {bias }}=V_{b}\right] \tag{4.28}
\end{align*}
$$

Similarly deriving the other sensitivities from the above equations, we get

$$
\begin{align*}
S_{V_{t_{n}}}^{I} & =\frac{V_{t_{n}}}{I} \frac{\partial I}{\partial V_{t}}=\frac{-2 I R}{V_{b}+I R-V_{t_{n}}}  \tag{4.29}\\
S_{\beta_{n}}^{I} & =\frac{\beta_{n}}{I} \frac{\partial I}{\partial \beta}=\frac{V_{b}-I R-V_{t_{n}}}{V_{b}+I R-V_{t_{n}}}  \tag{4.30}\\
S_{V_{t_{p}}}^{I} & =\frac{V_{t_{p}}}{I} \frac{\partial I}{\partial V_{t}}=\frac{-2 I R}{V_{b}+I R-V_{t_{p}}}  \tag{4.31}\\
S_{\beta_{p}}^{I} & =\frac{\beta_{p}}{I} \frac{\partial I}{\partial \beta}=1 \tag{4.32}
\end{align*}
$$

Now we consider the various noise currents present in the circuit, as shown in the figure 4.10.

$$
\begin{align*}
& \overline{i_{R_{1}}^{2}}=\left(\frac{4 K T}{R_{1}}\right) \Delta f \quad \text { and } \quad \overline{i_{R_{2}}^{2}}=\left(\frac{4 K T}{R_{2}}\right) \Delta f  \tag{4.33}\\
& \overline{i_{n_{1}}^{2}}=4 K T g_{m_{1}} \Delta f \quad \text { and } \overline{i_{n_{2}}^{2}}=4 K T g_{m_{2}} \Delta f  \tag{4.34}\\
& \overline{i_{n_{3}}^{2}}=4 K T y_{m_{3}} \Delta f \quad \text { and } \quad \overline{i_{n_{4}}^{2}}=4 K T g_{m_{4}} \Delta f \tag{4.35}
\end{align*}
$$



Figure 4.10 The various prominent noise current sources in interface cir-cuit-I

Assuming nominal values of $\Delta R=25 K \Omega$ and $C_{S D T}=50 f F$, the fastest RC switching time of the SDT bit would be $=25 \mathrm{~K} \Omega \times 50 \mathrm{fF}=800 \mathrm{Mhz}$. Assuming the noise bandwidth to be equal to this frequency, we have $\Delta f=800 \mathrm{Mhz}$. Also flicker (or) " $1 / \mathrm{f}$ " noise is neglected for both NMOS and PMOS transistors in the above calculations, due to the following reasons:

- NMOS: Due to source degeneration by SDT resistors, $g_{m}$ of these transistors and thus $g_{m}^{2} \overline{v_{n(1 / f)}^{2}}$ noise factor will be reduced. Hence we can neglect its ( $1 / \mathrm{f}$ ) contribution.
- PMOS: Due to current mirror configuration, we usually use bigger gate lengths and hence will have negligible (1/f) noise.

In order for the interface circuit to function properly, we should always have a positive signal current value and should satisfy certain conditions to meet the yield requirements.

For a given yield, the following condition has to hold true.

$$
\begin{align*}
\Rightarrow \Delta I_{\text {signal }} & \geq m \times \sigma_{\text {error, } \Delta I}  \tag{4.36}\\
\text { Now, } \quad \sigma_{\text {error, } \Delta I}^{2} & =\sum \sigma_{\text {error, } \Delta I_{i}}^{2} \\
\text { and in our case, we have } \frac{\sigma_{\Delta I_{\text {error }}}^{2}}{I^{2}} & =\frac{\sigma_{N M O S}^{2}}{I^{2}}+\frac{\sigma_{P M O S}^{2}}{I^{2}} \\
\text { Assuming, } \quad \sigma_{P M O S}^{2} & =K^{\prime} \sigma_{N M O S}^{2} \\
\Rightarrow \text { we get } \frac{\sigma_{\Delta I_{\text {error }}}^{2}}{I^{2}} & =\frac{\sigma_{N M O S}^{2}}{I^{2}}\left(1+K^{\prime}\right) \tag{4.37}
\end{align*}
$$

$$
\text { Now, } \begin{align*}
\sigma_{N M O S}^{2}= & \left(S_{v_{t}}^{I}\right)^{2} \sigma_{\Delta v_{t}}^{2}+\left(S_{\beta}^{I}\right)^{2} \sigma_{\frac{\Delta \beta}{\beta}}^{2}+\ldots \text { contd... } \\
& \ldots \text { contd... } 2 S_{v_{t}}^{I} \cdot S_{\beta}^{I} \cdot \sigma_{\Delta v_{t}} \cdot \sigma_{\Delta \frac{\Delta \beta}{\beta}} \cdot \rho\left(\Delta v_{t}, \frac{\Delta \beta}{\beta}\right)+\frac{\overline{i_{n o i s e}^{2}}}{I^{2}} \tag{4.38}
\end{align*}
$$

And, signal current, $\quad\left|\Delta I_{\text {signal }}\right|=\left|\frac{\partial I}{\partial R} \cdot \Delta R\right|=\frac{2 I^{2} \Delta R}{V_{b}+I R-V_{t}}$
Substituting equations $4.37,4.38$ and 4.39 in equation 4.36 , and solving them should give us an optimum operating condition for the interface circuit, satisfying the yield requirements for given mismatch parameters.

Appendix-B gives the $\operatorname{MATLA} B^{T M}$ code which implements the above described design procedure for interface circuit-I. This program solves the above equations 4.37,4.38 and 4.36, given the mismatch constants and noise parameters. The number of SDTs connected in series, for enhancing the produced signal, is passed on as a parameter to this program. It then predicts the expected yield for the interface circuit, given all these conditions. And for each predicted yield result, this program:

- Provides the appropriate NMOS/PMOS transistor sizes.
- Computes the optimum operating conditions (i.e) $V_{b i a s}, I_{\text {bias }}, I_{\text {Nominal }}$.
- Gives a choice to trade-off Output swing with transistor parameters.

Since the \# of SDTs used is parameterized, we can change the number of SDTs in series at anytime to enhance the yield and to affect the resultant transistor parameters.

Figures 4.11 and 4.12 show sample result graphs from this matlab routine. Figure 4.11 shows results computed for the case where \# of SDTs connected in series is one. As seen from the graph, the PMOS transistor parameters are traded off with respect to Output swing. While the NMOS transistor parameters are traded off with $V_{\text {bias }}$ operating condition. The user can then choose the appropriate operating conditions and their corresponding transistor parameters. Figure 4.12 shows similar results, but for an larger number of SDTs connected in series.

The computed yield values is also shown in the graphs. As expected, the predicted yield increases by significant amount, when the \# of SDTs connected in series is increased. The predicted yield is only a SOFT yield, which does not take into account wafer or die defects from processing steps. Hence the yield obtained from real fabricated circuits might be lesser than the predicted value.



Figure 4.11 Computed yield and transistor parameters for interface circuit-I with \# of SDTs $=1$



Figure 4.12 Computed yield and transistor parameters for interface circuit-I with \# of SDTs $=3$

## 5 EXPERIMENTAL RESULTS

In this section, two sets of measurement results will be presented. One set being the results of characterizing mismatches in the process used. While the other set will show the testing of various interface circuits designed.

### 5.1 Mismatch Measurement Results

Four dies were fabricated to measure the various mismatches present in both NMOS and PMOS transistors. Two dies were meant to characterize mismatches between identical transistors with variation in transistor sizes, while the other two dies were designed to measure the mismatches with variation in gate distance between identical transistors. HP4145B semiconductor parameter analyzer was used for all these tests.

The basic mismatch parameters of interest are the mismatch constants $\left\{A_{V_{t}}, A_{\beta}\right.$, $\left.A_{\gamma}, S_{V_{t}}, S_{\beta}, S_{\gamma}\right\}$ described in the equations (4.4) and (4.5) of chapter 4. In order to measure these constants, variances of the respective transistor parameter's $\left\{v_{t h}, \beta, \gamma\right\}$ mismatch has to be measured across the complete wafer. Moreover since differential pairs were designed for characterization, we also measured the offset voltage present in the differential pair.

The following would elaborate the measurement methods:

- Two sweep curves were measured on each transistor being characterized - $I_{d}$-vs- $V_{g s}$ and $I_{d}$-vs- $V_{s b}$. And Transistor parameters $\left\{V_{t h} \& \beta\right\}$ were measured as intercept and slope of $\sqrt{I_{d}}$-vs- $V_{g s}$ sweep curves.
- Transistor parameter f was measured by finding the difference in the intercepts of $\sqrt{I_{d}}$-vs- $V_{g s}$ curyes for various values of $V_{s b}$. This was accomplished by sweeping
the substrate potential through a SMU connector of HP4145B.
- Differential offset was measured by keeping both transistors of a pair in saturation and sweeping the gate voltages together while measuring the differences in their drain currents. The various voltages set for this test were : $V_{d s}=3.0 \mathrm{v}, V_{g s}=2.99$ $\rightarrow 3.01 \mathrm{v}, V_{s b}=0 \mathrm{v}$, from which the offset was measured as shown below [22]

$$
\begin{align*}
I_{d_{1}} & =m_{1} V_{g s}+n_{1} \\
I_{d_{2}} & =m_{2}\left(V_{g s}+V_{o f f s e t}\right)+n_{2} \\
\Rightarrow V_{\text {offset }} & =\frac{m_{1}-m_{2}}{m_{2}} V_{g s}+\frac{n_{1}-n_{2}}{m_{2}} \tag{5.1}
\end{align*}
$$

- For each pair of transistors, 8 dies (choosen around the wafer center to minimize large variations in transistor parameters) were tested across the wafer and thereby mean/variances were calculated from this set of 8 measured data.

Figure 5.1 shows the offset measurements for NMOS transistors. As seen from the graphs, offset voltage was measured as a function of variation in both transistor gate distances and transistor sizes. The top graph shows the measurements with variation in transistor gate distances and bottom graph shows the same for variation in transistor's size represented as $1 / \sqrt{W L}$ (where ' $W$ ' is the Width and 'L' the length of each measured transistor). Note that along with variance curve, the mean was also plotted for reference. Moreover, the circles in each graph represent the actual measured points from which a best line was computed and plotted. The offset voltage does seem to have the same characteristics as described by equations (4.4) and (4.5). The average offset voltage, which was computed as an average of all the measured mean values, is also shown in the graphs. This average value gives an estimate of the offset voltage that can be expected from differential pairs realized in TSMC $0.35 \mu$ process. A similar data for PMOS transistors is shown in fig 5.2.

Figure 5.3 shows the measured mean/variances of NMOS parameter mismatches. The left column of 3 graphs show the parameter variance/mean with respect to change in transistor size. While the right column show the parameter variance/mean with


Figure 5.1 Offset mismatch measurementsswant indabomatransistors
respect to change in transistor gate separation. The NMOS mismatch constants are derived from these graphs, whereby they are approximated to the slope of the best fit line through these measured data. Figure 5.4 shows similar results for PMOS parameter mismatches. Table 5.1 tabulates the various mismatch constants calculated from these measurements.

A couple of precautionary measures to be taken before making mismatch measurements:

- Make sure the drain current $\left(I_{d}\right)$ direction is the same when making measurements of the two transistors in the differential pair.


Figure 5.2 Offset mismatch measurements fobmitabobinatiansistors

- When making measurements of one transistor, make sure the other transistor in the pair is completely turned off - in order to prevent any leakage current. Connect all the nodes of the unused transistor to most negative supply voltage.
- Turn off any light source directly falling on the measured die. This is to make sure we do not inject any unwanted charges in the substrate.
- Use ferrite beads wherever necessary on the connectors to HP4145B SMUs, in order to prevent high-frequency noise being coupled onto drain current measurements.
- Use large integration times in HP4145B measurements to get a better averaged value of drain currents.

Table 5.1 Matching data for NMOS and PMOS transistors in a TSMC $0.35 \mu \mathrm{n}$-Well process

| parameter | nmos s.d. | pmos s.d | unit |
| :--- | :---: | :---: | :---: |
| $A_{V_{t}}$ | 3.99 | 16.71 | $\mathrm{mV} \mu \mathrm{m}$ |
| $A_{\beta}$ | 3.45 | 1.55 | $\% \mu m$ |
| $A_{\gamma}$ | $4.34 \times 10^{-3}$ | $13.45 \times 10^{-3}$ | $V^{0.5} \mu m$ |
| $S_{V_{t}}$ | 0.003 | 0.0177 | $\mu V / \mu m$ |
| $S_{\beta}$ | 3.804 | 2.687 | $10^{-6} / \mu m$ |
| $S_{\gamma}$ | 0.0078 | 0.0017 | $10^{-6} V^{0.5} / \mu m$ |

The above measurements of mismatch assumed a basic model (BSIM level-3 models) of transistor behavior and hence might not be the most accurate estimate of the process mismatches. In order to get a better evaluation, we have to use higher order non-linear curve-fitting methods to calculate the variance of each parameter that we are interested of. Due to lack of time, this methodology could not implemented. But those interested can refer [22] for further detailed explanations of this methodology.

### 5.2 Interface Circuits Measurement Results

The interface circuits could not be tested due to some unforeseen circumstances and hence experimental data is unavailable at this time for these circuits. Hybrid magnetic structures could not be made available by the sponsor, but attempts were made to realize traditional spiral-shaped tunnel junctions in place of the hybrid junctions. But unfortunately, due to some layout/mask errors in the tunnel junction lithography, connections to the underlying interface circuit was not realized. Hence even though the tunnel junctions were deposited, they were never connected to the underlying CMOS circuitry. These circuits are being re-fabricated with new deposition of tunnel junctions and hence future testing might reveal these circuit's performances.


Figure 5.3 NMOS transistor parameter mismatch measurements


Figure 5.4 PMOS transistor parameter mismatch measurements
Student Version of MATLAB

## 6 CONCLUSIONS

### 6.1 Summary

Monolithic memory cell structures with integrated SDT devices as non-volatile storage have been proposed. The structural and behavioral characteristics of the proposed interface circuits have been described and analyzed. The effects of process variations/mismatches on the circuit have been discussed. Also a methodology for designing these circuits for a given yield and a given process mismatch data has been proposed, along with automated matlab programs to aid in design process. Test circuits for these structures have been designed and fabricated in TSMC $0.35 \mu$ CMOS process with integrated SDT thin film technology. Also circuits to characterize the process mismatch were fabricated for both NMOS and PMOS transistors. Furthermore, wafer level tests have been conducted to characterize and tabulate the various process's mismatch factors.

### 6.2 Proposed Future Works

The interface circuits with both traditional tunnel junctions and Hybrid tunnel junctions is not yet available for evaluation. As soon as they become available, the first task will be to test and characterize the functionality of the proposed interface circuits.

A couple of design variations will be presented now, which can be further investigated and designed in the future.

### 6.2.1 Interface Circuit-III Variation

Mismatch analysis of this interface circuit showed a flaw in its design, wherein the shorting transistors were limiting the produced signal. And also this circuit was more susceptible to the mismatch in shorting transistors, more than to the mismatch variations of SDT resistors. But these problems can be easily fixed by a small change in the circuit topology, as shown in the figure 6.1. The bias voltage for the shorting transistors has been separated and hence by individually controlling each shorting transistor's bias voltage, we can actually override the mismatch present between those transistors. Moreover we can even enhance the produced SDT signal by properly choosing the bias voltages and thus also improve the circuit's response speed. This argument holds true even under the worst-case variations of SDT resistance. Nonetheless, the best advantage is that we can simply eliminate the mismatch present between the two shorting transistors.

### 6.2.2 Shadow D-FlipFlop

All the three designed latch structures can be used as a shadow memory along with a regular CMOS D-Latch. The non-volatile latch can be continuously written, whenever the output of the DFF changes. So this way; when the power is lost - the last written state in the DFF is retained in the non-volatile latch. And also, when the power is regained - the DFF can be restored to its last written state using the non-volatile latch data. Hence the data is never lost at any time. The functional block diagram of this scheme is shown in figure 6.2

### 6.2.3 8-bit Non-Volatile D-latch

The above mentioned Shadow D-Flipflop can also be used to construct a 8 -bit Nonvolatile latch/register. This design is similar to the commercial products - FM573 and FM574 - marketed by Ramtron International Corporation, based in Colorado springs, USA. Ramtron products are based upon on ferroelectric rams [23], which have limited number of write cycles and supposedly have large access times. By using our latch circuits, which are based upon spin tunneling junctions, we can overcome both those


Figure 6.1 Method to enhance the performance of interface circuit-III
limitations - since these magnetic bits have unlimited write endurance and produce large input signals, thus speeding up the access times. Such a design has potentially many applications like in control relays and valves with automatic setting on powerup without processor intervention. Interface to soft/momentary front panel switches \& indicator lamps, in Initializing state of I/O card signals and further more. These applications are possible because of this scheme's advantages - wherein it allows nonvolatile storage of data and system settings without the system overhead or extra pins of a serial memory. The power-on-reset modules in the circuit are meant to detect power up/down sequences and to bring the chip into the last stored state.

So far, only simple test circuits were implemented. In the future, larger systems with the proposed latch structures should be developed to further demonstrate the potential


Figure 6.2 Non-volatile latch used as a shadow memory
of these designs in different digital systems.

## APPENDIX A DIE LAYOUTS



Figure A. 1 Typical layout for mismatch characterization with transistor gate size variation


Figure A. 2 Typical Layout for mismatch characterization with transistor gate distance variation


Double gaurd ringed NMOS section

Figure A. 3 Layout of bit write circuitry


Figure A. 4 Layout of interface circuit-I


Figure A. 5 Layout of interface circuit-II

Double gaurd ringed PMOS section


Double gaurd ringed NMOS section
Figure A. 6 Layout of interface circuit-III


Figure A. 7 Die layout for mismatch characterizations


Figure A. 8 Die layout for the interface circuits

## APPENDIX B MATLAB PROGRAM CODE

## B. 1 Matlab Programming

Following is the matlab code for finding an optimum solution for the interface circuitI, to match a given yield under a given process mismatch data.

```
%******************************************************************
```

\% Interface Circuit-I solution

clear all;
close all;
format short E;
$\mathrm{f} 1=$ fopen('latch1_results','w'); \% Output file to store the calculated optimum results
$\operatorname{vdd}=3.3 ;$
Lov $=0.05 \mathrm{e}-6 ; \quad$ \% Overlap length - obtained from the MOSIS model file
$\mathrm{KT}=1.38 \mathrm{e}-23 * 290 ; \quad$ \% boltzman constant * temperature
$\mathrm{BW}=800 \mathrm{e} 6 ; \quad \quad \% 800 \mathrm{MHz}$ bandwidth for noise calculations
$\mathrm{m}=7.0 ; \quad$ \% number of sigmas for yield calculations
iterMAX $=100 ; \quad$ \% Max. number of iterations to find optimum solution
msplit $=0.9 ; \quad \%$ Initial split-up of the mismatch current between NMOS \& PMOS
NoOfSDTs $=3$; $\quad$ \% No of tunnel junctions in series
$R N=25 \mathrm{e} 3 ; \quad$ \% Nominal resistance of tunnel junctions
$\mathrm{kmin}=15 \mathrm{e}-2$;
knom $=15 \mathrm{e}-2$;
$\operatorname{kmax}=25 \mathrm{e}-2 ;$
\% Minimum SDT magnetoresistance
\% Nominal SDT magnetoresistance
\% Maximum SDT magnetoresistance

Avtn $=3.99 \mathrm{e}-3 * 1 \mathrm{e}-6 ; \quad \%$ Transistor size related Mismatch constant for $V_{t h}-$ NMOS Avtp $=16.712 \mathrm{e}-3^{*} 1 \mathrm{e}-6 ; \%$ Transistor size related Mismatch constant for $V_{t h}$ - PMOS Abetan $=3.45 \mathrm{e}-2$ * $1 \mathrm{e}-6 ; \quad \%$ Transistor size related Mismatch constant for $\beta$ - NMOS Abetap $=1.55 \mathrm{e}-2 * 1 \mathrm{e}-6 ; \quad \%$ Transistor size related Mismatch constant for $\beta-\mathrm{PMOS}$ Agamman $=4.34 \mathrm{e}-2 * 1 \mathrm{e}-6 ; \%$ Transistor size related Mismatch constant for $\gamma-$ NMOS Agammap $=13.45 \mathrm{e}-2 * 1 \mathrm{e}-6 ; \quad \%$ Transistor size related Mismatch constant for $\gamma-$ PMOS

Athetan $=10 \mathrm{e}-2^{*} 1 \mathrm{e}-6 ; \quad \%$ Transistor size related Mismatch constant for $\theta$ - NMOS Athetap $=5 \mathrm{e}-2^{*} 1 \mathrm{e}-6 ; \quad \%$ Transistor size related Mismatch constant for $\theta$ - PMOS
rho1n $=-0.35 ;$
rholp $=0.25$;
rho2n $=0.5$;
rho2p $=0.2$;
rho3n $=-0.5$;
rho3p $=-0.5$;
rho4n $=0.971$;
rho4p $=0.978$;
$\mathrm{phi}=0.7$;
$\operatorname{vtn} 0=0.536 ;$
$\operatorname{vtp} 0=0.735 ;$
gamman $=0.5$;
gammap $=0.5$;
$\mathrm{k} \_\mathrm{n}=100 \mathrm{e}-6$;
$k_{\_} \mathrm{p}=44 \mathrm{e}-6$;
mu_n $=0.05$;
mu_p $=0.02$;
tox $=7.7 \mathrm{e}-9$;
Cox $=3.9$ * $8.854 \mathrm{e}-12 /$ tox ;
$\mathrm{dRmin}=\mathrm{kmin} * \mathrm{RN}$;
$\%$ correlation between $v_{t_{n}}$ and $\beta_{n}$ $\%$ correlation between $v_{t_{p}}$ and $\beta_{n}$ $\%$ correlation between $v_{t_{n}}$ and $\gamma_{n}$ $\%$ correlation between $v_{t_{p}}$ and $\gamma_{p}$ $\%$ correlation between $\beta_{n}$ and $\gamma_{n}$ $\%$ correlation between $\beta_{p}$ and $\gamma_{p}$ $\%$ correlation between $\beta_{n}$ and $\theta_{n}$ $\%$ correlation between $\beta_{p}$ and $\theta_{p}$ \% substrate potential \% Nominal threshold voltage of NMOS \% Nominal threshold voltage of PMOS \% NMOS substrate threshold factor \% PMOS substrate threshold factor

$$
\begin{array}{r}
\%\left(\mu_{n} \times C_{o x}\right) / 2 \\
\left.\% \mu_{p} \times C_{o x}\right) / 2
\end{array}
$$

\% mobility factor for NMOS \% mobility factor for PMOS \% Gate oxide thickness \%Unit gate capacitance \%Minimum value of magnetoresistance

```
dRnom = knom * RN;
dRmax = kmax * RN;
```

\%Nominal value of magnetoresistance
\%Maximum value of magnetoresistance

## $\%^{* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * ~}$

\% step 1: calculate the maximum bias current, INmax


INmax $=$ NoOfSDTs * 150e-3/(2*RN*(1 $+\mathrm{kmax} / 2)$ );
IN = INmax

\% step 2 : calculate the signal current, DeltaIN \& YIELD calculations

for $\mathrm{msplit}=0.1: 0.1: 0.9$

$$
\begin{aligned}
& \mathrm{m}=7.0 \\
& \text { iter }=0 \\
& \mathrm{vtn}=\mathrm{vtn} 0+\operatorname{gamman}^{*}\left(\operatorname{sqrt}\left(\mathrm{phi}+I N^{*} \mathrm{RN}\right)-\operatorname{sqrt}(\operatorname{phi})\right)
\end{aligned}
$$

$$
\text { start } 1=\mathrm{IN}^{*} \mathrm{RN}+\mathrm{vtn}+0.2 ; \% \mathrm{~min} \text { bias voltage required for } 200 \mathrm{mv} \text { of vdsat }
$$

$$
\text { stop1 }=3
$$

$$
\text { stop } 1=3
$$

$$
\text { nflag1 = } 0
$$

$$
\text { nflag2 }=0 ;
$$

$$
\text { breakflag1 }=0
$$

$$
\text { nmostrueflag }=0
$$

$$
\operatorname{cnt} 1=0
$$

$$
\text { endflag1 = } 0
$$

$$
\mathrm{vtp}=\mathrm{vtp} 0
$$

$$
\text { start2 }=\mathrm{vdd} / 2-0.5
$$

$$
\text { stop } 2=\mathrm{vdd} / 2+0.5
$$

$$
\text { stop2 }=\text { stop2; }
$$

$$
\text { pflag1 }=0
$$

```
pflag2 = 0;
breakflag2 = 0;
pmostrueflag = 0;
cnt2 = 0;
endflag2 = 0;
while (iter }\leq\mathrm{ iterMAX)
for i = 1:1:500
    vbias(i)}=\operatorname{start1}+(\mathrm{ stop1 - start1)}\mp@subsup{*}{\textrm{i}}{2}/500
    term1 = gamman /sqrt(phi+IN*RN);
    dIN}(\textrm{i})=(2*IN*IN* (1+term1)*dRnom)/(vbias(i) + IN*RN - vtn +
2*IN*RN*
    dINmin}(\textrm{i})=(2*IN*IN* (1+term1)*dRmin )/(vbias(i) + 2*IN*RN - vtn +
2*IN*RN*term1);
S_I_vtn = -2*vtn/(vbias(i) +IN*RN - vtn + 2*IN*RN*term1);
S_I_betan = (vbias(i) - IN*RN - vtn ) /(vbias(i) + IN*RN - vtn + 2*IN*RN*term1);
S_I_gamman =-2*(vtn - vtn0) /(vbias(i) +IN*RN - vtn + 2*IN*RN*term1);
sigmasq_vtn = ((S_I_vtn * Avtn)\hat{2})/(vtn\hat{2});
sigmasq_betan = (S_I_betan * Abetan)}\hat{2}
sigmasq_gamman = (S_I_gamman * Agamman)}\hat{2}
corr_vtn_betan =2 * S_I_vtn * S_I_betan * Avtn * Abetan * rho1n/vtn;
corr_vtn_gamman =2 * S_I_vtn * S_I_gamman * Avtn * Abetan * rho2n/vtn;
corr_betan_gamman =2 * S_I_betan * S_I_gamman * Abetan * Agamman * rho3n;
isq_noise_sdt =2*(4*KT*(1/RN)*BW); % two SDT resistors
gmx = 2*IN/(vbias(i) - IN*RN - vtn);
isq_noise_nmos = 2* (4*KT* gmx*BW);
isq_noise(i) = isq_noise_sdt + isq_noise_nmos;
sigmasq_errordIN}(\textrm{i})=m\mp@code{mslit * ((dINmin}(\textrm{i})/\textrm{m})\hat{2}-\mathrm{ isq_noise_sdt })\mathrm{ ;
num(i) = sigmasq_vtn + sigmasq_betan + sigmasq_gamman + corr_vtn_betan +
corr_vtn_gamman + corr_betan_gamman;
```

$\mathrm{WLn}(\mathrm{i})=\mathrm{IN}^{*} \mathrm{IN}^{*}($ num(i) $) /($ sigmasq_errordIN(i) - isq_noise_nmos $) ;$
den $(\mathrm{i})=$ sigmasq_errordIN(i) - isq_noise_sdt - isq_noise_nmos;
$\mathrm{W} \operatorname{Ln}(\mathrm{i})=\mathrm{IN} /\left(\mathrm{k} \_\mathrm{n}^{*}(\operatorname{vbias}(\mathrm{i})-\mathrm{IN} * \mathrm{RN}-\mathrm{vtn}) \hat{2}\right) ;$
$\operatorname{Ln}(\mathrm{i})=\operatorname{sqrt}\left(\mathrm{WLn}(\mathrm{i}) / \mathrm{W} \_\operatorname{Ln}(\mathrm{i})\right) ;$
$\mathrm{Wn}(\mathrm{i})=\mathrm{WLn}(\mathrm{i}) / \operatorname{Ln}(\mathrm{i}) ;$
end
if (nflag1 $==0$ )
sti $=1 ;$ endi $=500 ;$
for $\mathrm{i}=2: 1: 500$
if $(\operatorname{den}(\mathrm{i}) \geq 0) ; \mathrm{nflag} 1=1$; end
if $((\operatorname{den}(\mathrm{i}-1) \leq 0) \hat{(\operatorname{den}(\mathrm{i}) \geq 0)})$; sti $=\mathrm{i} ;$ nflag $1=1$; end
if $((\operatorname{den}(i-1) \geq 0) \hat{(\operatorname{den}(i) \leq 0)}$; endi $=\mathrm{i}-1$; nflag $1=1$; end
end
if $(($ nflag $1==0)-($ endi $==s t i))$
$\mathrm{m}=\mathrm{m}-0.2 ; \mathrm{nflag} 1=0 ; \mathrm{nflag} 2=0 ; \mathrm{pflag} 1=0 ; \mathrm{pflag} 2=0 ; \operatorname{cnt} 1=0 ; \operatorname{cnt} 2=0 ;$
if $(\mathrm{m} \leq 0.2)$; breakflag $1=1$; nflag $1=0$; end
elseif (endi $\geq$ sti)
start1 $=\operatorname{vbias}($ sti $) ;$ stop $1=\operatorname{vbias}($ endi $) ;$ cnt1 $=\mathrm{cnt} 1+1 ;$
if ( cnt1 $\leq 2$ ); nflag1 $=0$; end
if (cnt1 $==2$ ); cnt1 $=0$; end;
end
end
if (breakflag1 ==1); break; end
if $(($ nflag $1==1) \hat{(e n d i} \geq s t i))$
sti2 $=$ sti; endi2 $=$ endi;
for $\mathrm{i}=$ sti:1:endi-1
if $((\operatorname{Ln}(\mathrm{i}) \leq 10 \mathrm{e}-6) \hat{(\operatorname{Ln}(\mathrm{i})} \geq 0.35 \mathrm{e}-6) \hat{(\mathrm{nflag} 2}==0))$
if $(\mathrm{Wn}(\mathrm{i}) \geq 0.4 \mathrm{e}-6)$; sti2 $=\mathrm{i}$; nflag2 $=1$; end
end
if $((\operatorname{Ln}(\mathrm{i}) \geq 10 \mathrm{e}-6) \hat{(\operatorname{Ln}(\mathrm{i}+1)} \leq 10 \mathrm{e}-6) \hat{(\mathrm{nflag} 2}==0))$
if $(\mathrm{Wn}(\mathrm{i}) \geq 0.4 \mathrm{e}-6) ;$ sti2 $=\mathrm{i}+1$; nflag2 $=1$; end
end
if $((\operatorname{Ln}(\mathrm{i}) \leq 10 \mathrm{e}-6) \hat{(\operatorname{Ln}(\mathrm{i}+1)} \geq 10 \mathrm{e}-6) \hat{(\mathrm{nflag} 2}==1))$
if $(\mathrm{Wn}(\mathrm{i}) \geq 0.4 \mathrm{e}-6)$; endi2 $=\mathrm{i}$; end
end
end
if $(($ nflag $2==0)-($ endi $2==$ sti2 $))$
$\mathrm{m}=\mathrm{m}-0.2$;
sprintf('\%s \%d','in NMOS loop1 with endflag1 = ',endflag1);
nflag1 $=0 ;$ nflag2 $=0 ;$ pflag1 $=0 ;$ pflag2 $=0 ; \operatorname{cnt} 1=0 ; \operatorname{cnt} 2=0 ;$
if ( $\mathrm{m} \leq 0.2$ ); breakflag $1=1$; end
elseif (nflag2 ==1)
start1 $=\operatorname{vbias}($ sti2 $) ;$ stop $1=\operatorname{vbias}($ endi2 $) ; \operatorname{cnt} 1=\mathrm{cnt} 1+1 ; \mathrm{m} ;$
cnt1;
endflag1;
if (cnt1 $\leq 2$ ); nflag2 $=0$; end
if $(\operatorname{cnt1}==2) ;$ nmostrueflag $=1 ;$ endflag $1=1 ; \operatorname{cnt} 1=0 ;$ nflag $1=0 ;$ nflag2 $=0$;
sprintf('\%s \% d','satisfied NMOS with endflag1 = ',endflag1);
else nmostrueflag $=0$; endflag $1=0$ : end
end
end
if (breakflag1 $==1$ ); break; end

## \%*

\% step 4: PMOS parameters

```
%****************************************************************
```

for $\mathrm{i}=1: 1: 500$

$$
\operatorname{vout}(\mathrm{i})=\operatorname{start} 2+(\operatorname{stop} 2-\operatorname{start} 2) * \mathrm{i} / 500
$$

$$
\text { S_I_vtp } \left.=-2^{*} v t p /(v d d-\operatorname{vout}(i)-v t p)\right)
$$

```
    S_I_betap \(=1\);
    sigmasq_vtp \(=((\) S_I_vtp \(*\) Avtp \() \hat{2}) /(v t p \hat{2}) ;\)
    sigmasq_betap \(=(\) S_I_betap \(*\) Abetap \() \hat{2}\);
    corr_vtp_betap \(=2\) * S_I_vtp * S_I_betap * Avtp * Abetap * rholp/vtp;
    \(g m x=2 * I N /(v d d-\operatorname{vout}(i)-v t p) ;\)
    isq_noise_pmos \(=2^{*}\left(4^{*} \mathrm{KT}^{*} \mathrm{gmx}{ }^{*} \mathrm{BW}\right)\);
    isq_noise_sdt \(=2^{*}\left(4^{*} \mathrm{KT}^{*}(1 / \mathrm{RN}) * \mathrm{BW}\right) ; \%\) two SDT resistors
    sigmasq_errordIP \((\mathrm{i})=(1-\mathrm{msplit}) *((\mathrm{dINmin}(\mathrm{i}) / \mathrm{m}) \hat{2}\) - isq_noise_sdt \()\);
    WLp \((\mathrm{i})=\) IN \(^{*}\) IN* \({ }^{*}(\) sigmasq_vtp + sigmasq_betap +
corr_vtp_betap)/(sigmasq_errordIP(i) - isq_noise_pmos);
    \(\operatorname{denp}(\mathrm{i})=\) sigmasq_errordIP \((\mathrm{i})\) - isq_noise_pmos;
    W _Lp \((\mathrm{i})=\mathrm{IN} /\left(\mathrm{k} \_\mathrm{p} *(\mathrm{vdd}-\operatorname{vout}(\mathrm{i})-\mathrm{vtp}) \hat{2}\right) ;\)
    \(\operatorname{Lp}(\mathrm{i})=\operatorname{sqrt}\left(\mathrm{WLp}(\mathrm{i}) / \mathrm{W}_{-} \operatorname{Lp}(\mathrm{i})\right) ;\)
    \(\mathrm{Wp}(\mathrm{i})=\mathrm{WLp}(\mathrm{i}) / \operatorname{Lp}(\mathrm{i}) ;\)
    \(\operatorname{cgs} 1=2 / 3 * \mathrm{Wp}(\mathrm{i}) * \operatorname{Lp}(\mathrm{i}) * \operatorname{Cox}\);
    \(\operatorname{cgd} 1=\mathrm{Wp}(\mathrm{i}) *\) Lov * Cox;
    \(\operatorname{cd} 3=\mathrm{Wn}(\mathrm{i}){ }^{*}\) Lov \({ }^{*}\) Cox;
    delay \((\mathrm{i})=2^{*}\left(\left(2^{*} \operatorname{cgs} 1+\operatorname{cgd} 1+\operatorname{cd} 3\right) / \operatorname{gmx}+(\operatorname{cd} 3+\operatorname{cgd} 1) / \mathrm{IN}\right) ;\)
    vds_drop(i) \(=\) vdd \(-\operatorname{vout}(i)-I N * R N\);
end
iter \(=\) iter \(+1 ;\)
if (pflagl \(==0\) )
    endflag2 \(=0\);
    sti \(=1 ;\) endi \(=500 ;\)
    for \(i=2: 1: 500\)
    if \((\operatorname{denp}(\mathrm{i}) \geq 0)\); pflag1 \(=1\); end
    if \(((\operatorname{denp}(\mathrm{i}-1) \leq 0) \hat{(\operatorname{denp}(\mathrm{i}) \geq 0)})\); sti \(=\mathrm{i}\); pflag1 \(=1\); end
    if \(((\operatorname{denp}(\mathrm{i}-1) \geq 0) \hat{(\operatorname{denp}(\mathrm{i}) \leq 0)})\); endi \(=\mathrm{i}-1\); pflag \(1=1\); end
```

    end
    if $(($ pflag $1==0)-($ endi $==s t i))$
$\mathrm{m}=\mathrm{m}-0.2 ;$ nflag1 $=0 ;$ nflag2 $=0 ;$ pflag1 $=0 ;$ pllag2 $=0 ; \operatorname{cnt} 1=0 ; \operatorname{cnt} 2=0 ;$
if ( $\mathrm{m} \leq 0.2$ ); breakflag2 $=1$; end
elseif (endi $\geq$ sti)
start2 $=\operatorname{vout}($ sti $) ;$ stop $2=\operatorname{vout}($ endi $) ; \operatorname{cnt} 2=\operatorname{cnt} 2+1 ;$
if $($ cnt2 $\leq 2)$; pflag1 $=0$; end
if $(\operatorname{cnt} 2==2)$; cnt $2=0$; end;
end
end
if (breakflag2 ==1); break; end
if $(($ pflag $1==1) \hat{(e n d i} \geq$ sti $))$
sti2 $=$ sti; endi2 $=$ endi;
for $\mathrm{i}=$ sti:1:endi-1
if $((\operatorname{Lp}(\mathrm{i}) \leq 10 \mathrm{e}-6) \hat{(L p}(\mathrm{i}) \geq 0.35 \mathrm{e}-6) \hat{(p f l a g} 2==0))$
if $(\mathrm{Wp}(\mathrm{i}) \geq 0.4 \mathrm{e}-6) ;$ sti2 $=\mathrm{i}$; pflag2 $=1$; end
end
if $((\operatorname{Lp}(\mathrm{i}) \geq 10 \mathrm{e}-6) \hat{(\mathrm{Lp}}(\mathrm{i}+1) \leq 10 \mathrm{e}-6) \hat{(p f l a g} 2==0))$
if $(\mathrm{Wp}(\mathrm{i}) \geq 0.4 \mathrm{e}-6) ;$ sti2 $=\mathrm{i}+1 ;$ pflag2 $=1$; end
end
if $((\operatorname{Lp}(\mathrm{i}) \leq 10 \mathrm{e}-6) \hat{(\mathrm{Lp}}(\mathrm{i}+1) \geq 10 \mathrm{e}-6) \hat{(p f l a g} 2==1))$
if $(\mathrm{Wp}(\mathrm{i}) \geq 0.4 \mathrm{e}-6)$; endi2 $=\mathrm{i}$; end
end
end
if $(($ pflag $2==0)-($ endi $2==$ sti 2$))$
$\mathrm{m}=\mathrm{m}-0.2$;
sprintf('\%s \%d','in pmos loop with endflag2 = ',endflag2);
nflag1 $=0 ;$ nflag2 $=0 ;$ pflag2 $=0 ;$ pflag $1=0 ; \operatorname{cnt} 1=0 ; \operatorname{cnt} 2=0 ;$
if ( $\mathrm{m} \leq 0.2$ ); breakflag2 $=1$; end
elseif (pflag2 $==1$ )
start2 $=\operatorname{vout}($ sti2 $) ;$ stop $2=\operatorname{vout}($ endi2 $) ;$ cnt $2=\operatorname{cnt} 2+1 ; \mathrm{m} ;$
cnt2;
endflag2;
if $($ cnt2 $\leq 2)$; pflag2 $=0$; end
if (cnt2 $==2$ ); pmostrueflag $=1$; endflag2 $=1 ;$ cnt2 $=0 ;$ pflag1 $=0 ;$ pflag2 $=0$;
sprintf('\%s \%d','satisfied PMOS with endflag2 =',endflag2);
else pmostrueflag $=0$; endflag2 $=0$; end
end
end
if (breakflag2 $==1$ ); break; end
if $(($ endflag $1==1)$ (endflag2 $==1)$; break; end
end
yield $=100^{*}(\operatorname{erf}(\mathrm{~m} / \operatorname{sqrt}(2)))$;
end

$\%$ step 5: results display
$\%$
fclose(f1);
figure
plot(vbias,den);
xlabel('vbias');
ylabel('difference between noise factors and error current');
grid on;
figure;
$\mathrm{ax}=$ plotyy(vbias,WLn,vbias,W_Ln);
xlabel('vbias');
axes(ax(1));
axis tight;
ylabel('WL product');
axes(ax(2));
axis tight;
ylabel('W/L ratio');
grid on;
figure
$h 1=\operatorname{plot}(v b i a s, W n, ' r ') ;$
hold on
$\mathrm{h} 2=\operatorname{plot}\left(\right.$ vbias,Ln, ${ }^{\prime} \mathrm{b}$ ');
grid on;
axis tight;
legend([h1 h2],'Width', 'Length');
xlabel('vbias');
ylabel('NMOS transistor parameters');
$\mathrm{sl}=\operatorname{sprintf(}$ ('\%s \%d $\% \mathrm{~s} \% \mathrm{~d} \% \mathrm{~s} \% \mathrm{~d}$ ','msplit=',msplit,'m=',m,'yield=',yield);
title(s1);
figure
$\mathrm{h} 1=\operatorname{plot}\left(\right.$ vout, $\left.\mathrm{Wp}, \mathrm{r}^{\prime}\right)$;
hold on
$\mathrm{h} 2=\operatorname{plot}\left(\right.$ vout,Lp, $\left.{ }^{\prime} \mathrm{b}^{\prime}\right)$;
grid on;
axis tight;
legend([h1 h2],'Width','Length');
xlabel('vout');
ylabel('PMOS transistor parameters');
$\mathrm{s} 1=\operatorname{sprintf(}$ ( $\% \mathrm{~s} \% \mathrm{~d} \% \mathrm{~s} \% \mathrm{~d} \% \mathrm{~s} \% \mathrm{~d}^{\prime}$, 'msplit=',msplit,'m=',m,'yield=',yield); title(s1);

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